# GPST Topic 1: Advanced inverter applications (and requirements) for current-limited grid-forming inverters

2022 CSIRO GPST Research

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# Executive Summary

This project presents a comprehensive study of grid-forming inverters in power systems, focusing on their design, transient stability, and control enhancements. The research aims to improve the performance and reliability of inverter-based resources (IBRs) as they become increasingly prevalent in modern power systems. The research project consists of several interconnected tasks, progressing from inverter design specifications to the analysis of complex multi-IBR systems.

The research begins with a thorough review of global grid codes and performance standards to derive inverter design specifications that enhance their ability to remain connected to the grid during large signal events. This foundation enables the investigation of transient stability in grid-forming inverters (GFMIs) equipped with current limiters, which are necessary to protect GFMIs from overcurrents, but degrade the stability margin of GFMIs. The study emphasises the importance of q-prioritised current limiters, which are commonly employed in the industry.

Building on these insights, the research explores the transient stability of paralleled systems, including grid-forming and grid-following inverters. This analysis leads to the development of an adaptive power reference control (APRC), designed to enhance transient stability in various scenarios. Experimental testbench evaluations at Monash University demonstrate the effectiveness of the APRC in improving the damping and stability of the grid-forming inverters.

Subsequently, the research extends its focus to multi-inverter-based resource systems. The goal is to develop indices or indicators that allow for quick measurement of transient stability margins, taking into account the distance between stable and unstable equilibrium points in the system's operating domain. This analysis aims to provide a practical tool for evaluating the performance and stability of complex power systems with multiple IBRs. The output of the tool can provide indicators for the transient stability margin of a network. Within this stage (stage 2), some preliminary studies in developing the analysis behind the tool have been conducted. In the next stage (stage 3), the development of the tool will continue to extend its capability and improve the computing process.

Overall, this research contributes knowledge and analysing tools for designing, operating, and controlling grid-forming inverters in modern power systems. The findings in this project can help original equipment manufacturers (OEMs) and IBR developers quickly determine the stability limits of a GFMI when connecting it to a given point of connection. This allows a proper design of the GFMI and understanding the capability of the inverter. Furthermore, the enhancing controllers proposed and investigated in this stage can be used as recommendations for OEMs to further improve the robustness of their GFMI models. The results not only improve the transient stability of these systems but also ensure reliable grid integration as renewable energy resources continue to expand.

Percentages of the research plan tasks that have been completed in the 2022/23 Stage 2 work:

- Enhancing IBR response during and subsequent to faults (Urgent topic) – 40%
- Developing alternative control methodologies for GFMIs – 25%

List of tasks:

- Inverter Design Specifications
- Transient Stability of GFMIs in the Presence of Current Limiters
- Transient Stability of Paralleled GFMI-GFLI Systems
- Transient Stability Analysis for Multi-IBR Systems
- Transient Stability Enhancing Methods
- GFMI's Functionality Tests

# Acknowledgement

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# Glossary

| Term | Definition |
|---|---|
| Active power controller (APC) | The active power controller of a GFMI. |
| Adaptive power reference control (APRC) | An enhancing controller, presented in Section 2.4.1, that adaptively adjusts the power reference of a VSG to improve the transient stability of the VSG. |
| Critical clearing time (CCT) | The maximum amount of time to clear a fault on the system and restore stable operation. |
| Current limiter (CL) | A component in GFMI control system to protect the semiconductor inside the GFMI from overcurrent. |
| Deceleration volume (DV) | A stability margin indicator introduced in Section 2.3. |
| Distance between the stable equilibrium point and the unstable equilibrium point ($D_{\mathrm{EP}}$) | A stability margin indicator introduced in Section 2.5. |
| d-prioritised current limiter (d-CL) | A current limiter that sets the priority to the direct-axis current, leaving the remaining amount of available current headroom to the quadrature-axis current |
| During-fault current-limited (DF-CLd) | The power-angle curve in the current-limited mode of a VSG during a fault, studied in Section 2.2.3. |
| Equal-area criterion (EAC) | A graphical method used to determine the stability of a power system by analysing the area under the power-angle curve before and after a disturbance. |
| Equilibrium point | The state where all forces, inputs, and outputs balance each other, resulting in a stable and unchanging system behaviour. |
| Fault-ride through (FRT) | The ability of generators or other power electronic devices to remain connected and operational during short-term faults or disturbances on the grid, without causing further system instability. |
| Grid following inverter (GFLI) | A power electronic device that adjusts its output to match the voltage and frequency of the grid it is connected to, enabling it to feed power into the grid. |
| Grid forming inverter (GFMI) | A power electronic device that can autonomously generate and regulate both voltage and frequency in a grid. |
| Grid-forming battery energy storage system (GF-BESS) | A battery energy storage system interfaced with the grid via grid-forming inverters |
| Inverter-based resource (IBR) | A power generation or storage device that uses power electronic inverters to convert DC power into AC power, such as solar panels or battery storage systems. |
| Modified q-prioritised current limiter (mod-q-CL) | A modified model of the q-prioritised current limiter, presented in Section 2.4.2. |
| Negative-sequence (NS) | The presence of an unbalanced condition in which the phase voltages and currents have equal magnitudes but a 120-degree phase shift. |
| Normal-voltage current-limited (NV-CLd) | The power-angle curve in the current-limited mode of a VSG at a normal grid voltage level, studied in Section 2.2.3. |
| Normal-voltage voltage-controlled (NV-VC) | The power-angle curve in the voltage-controlled mode of a VSG, studied in Section 2.2.3. |

| | |
|---|---|
| Phase-locked loop (PLL) | A control mechanism that synchronises the phase angle and frequency of a power-electronics-based device with the voltage and frequency of the grid, providing stable and reliable operation. |
| Point of connection (PoC) | The physical location where an electrical device or system is connected to the grid. |
| Power-angle curve | A graph that represents the relationship between the power angle and the active power output of the generator, indicating the stability of the generator under different operating conditions. |
| q-prioritised current limiter (q-CL) | A current limiter that sets the priority to the quadrature-axis current, leaving the remaining amount of available current headroom to the direct-axis current |
| q-prioritised current-limited virtual synchronous generator (q-CL-VSG) | Virtual synchronous generator equipped with a q-prioritised current limiter |
| Root Mean Square (RMS) | The effective value of an AC voltage or current, representing the equivalent DC voltage or current that would produce the same average power. |
| Single-Machine Infinite Bus (SMIB) | A simplified model used to analyse the dynamic behaviour of a single generator connected to an infinite bus, representing the behaviour of an entire power system. |
| Stable equilibrium point (SEP) | A state where disturbances from this point will cause the system to return to the original state, indicating a robust and reliable system behaviour. |
| Synchronous generator (SG) | An electrical machine that converts mechanical energy into electrical energy, producing AC power that is synchronised with the frequency and voltage of the power system |
| The Electric Power Research Institute (EPRI) | An American independent, non-profit organization that conducts research and development related to the generation, delivery, and use of electricity. |
| Transient stability | The ability of a system to maintain synchronising with the grid after experiencing a large disturbance, such as a fault, without collapsing completely. |
| Unstable equilibrium point (UEP) | A state where disturbances from this point will cause the system to move away from the original state, indicating an unreliable system behaviour |
| Virtual synchronous generator (VSG) | A type of grid-forming inverter that can provide virtual inertia. |

# 1. Introduction

Grid-forming inverter (GFMI) is a type of power electronic device that converts direct current (DC) electricity into alternating current (AC) electricity and helps to form and regulate the electrical grid. It plays a crucial role in enabling the integration of renewable energy sources into the existing power grid and ensuring a stable and reliable power supply. The grid-forming inverter has the ability to synchronize with the grid and maintain a stable voltage and frequency, making it an essential component in modern power systems.

Due to the promising applications of GFMIs in the power system, their stability should be investigated so that their operational limits are determined and solutions can be proposed to improve their stability [1]. As the power system is vulnerable during faults and fault recoveries, studying the transient stability of GFMIs and their impacts on the networks during such events is necessary. Transient stability of GFMIs refers to the ability of the inverter to maintain its synchronisation with the grid and continue supplying power during and after disturbances, such as faults, voltage dips, or short-term interruptions. This is an important aspect of the inverter's behaviour in a microgrid or a larger power system, as it affects the overall stability and reliability of the power system. Transient stability of GFMIs is achieved by the careful design of control algorithms and protection schemes that ensure quick and appropriate responses to disturbances. In order to design a robust control scheme against large transient events, the limits and stability boundaries of GFMIs and the connected system need to be investigated first.

In this project, various studies are being conducted to both analyse and enhance the transient stability of GFMIs and the connected network during faults and fault recoveries. The tasks that have been conducted in this stage are introduced below.

- *Inverter Design Specifications: A review of grid codes and performance standards:* A white paper has been prepared to summarise requirements for transmission connected inverter-based resources (IBRs). This document provides a summary of requirements on the fault ride-through (FRT) capability of inverter-based resources, gathered from various grid codes. In addition, general recommendations for inverter design are also given in this document to minimise the negative impacts of system faults on the stability of IBRs and the connected system. The recommendation in prioritising reactive current during faults has been considered and carefully investigated in other tasks. In addition, different priority-based current limiters presented in this paper are benchmarked in the functionality tests below, with respect to grid codes summarised in this white paper. Furthermore, the standard IEEE P2800 mentioned in this white paper provided a guideline to design the negative-sequence current controller below.
- *Transient Stability of GFMIs in the Presence of Current Limiters:* As GFMIs are power electronic converters, they are sensitive to overcurrent, due to the limited thermal capability of the internal switches and their voltage-source-like operation, during and subsequent to large disturbances. Thus, GFMIs are always equipped with a current limiter (CL) in their control system to protect themselves from overcurrent. The engagement of CLs in the GFMI's control can significantly affect the operation of GFMIs and negatively impact GFMIs' stability. Therefore, in this project, the impacts of CLs on the transient stability of GFMIs have been investigated. The outcomes of this study reveal the instability mechanism and a new stability angle limit of a current-limited GFMI. This angle limit is the angle value where the vector voltage

controller starts becoming unstable. Based on these, a more accurate angle limit, that considers the stability of the voltage control loop, for GFMIs can be estimated.

- *Transient Stability of Paralleled GFMI-GFLI Systems:* In addition to the stability study of GFMIs, GFMI's impacts on nearby IBRs have also been analysed in this project. This study is necessary as grid-forming battery-energy-storage systems (GF-BESSs) are currently being installed in IBR-dominated areas of the power system to improve the grid strength of these areas and support grid-following-inverter-based (GFLI-based) IBRs there. This study allows understanding the stability boundary and stability margin of a paralleled GFLI-GFMI system. These understandings are beneficial for tuning the control parameters of the IBRs.
- *Transient Stability Analysis for Multi-IBR Systems:* The basics developed in the transient study of the paralleled GFMI-GFLI system have been extended to a larger system, which consists of multiple IBRs (four IBRs). In this study, an index, which indicates how stable a multi-IBR system is, in terms of transient stability, is proposed. This index can be useful in the dispatch planning process of the multi-IBR system. The power setpoint of the IBRs should be set so that the index is maintained above a certain threshold value. The threshold value can be set to the index of a stable network snapshot. By this approach, the stability margin of the network is kept above a desired level. Some preliminary studies in developing the analysis behind the tool have been conducted for a four-IBR system in this stage. In the next stage (stage 3), the development of the tool will continue to extend its capability and improve the computing process.
- *Transient Stability Enhancing Methods:* The understandings gained from the above studies are the foundations for designing a system that is robust against faults. Solutions to enhance the transient stability of GFMIs are also the outcomes of this project. So far, several enhancing controls have been proposed or investigated in this project to improve the transient stability margin of GFMIs and the connected networks during large transients, including Adaptive Power Reference Control (APRC), Modified q-Prioritised Current Limiter, and Freezing Active Power Control Loop During Faults. Improvements brought by these methods have been validated in PSCAD/EMTDC and experimentally as well.

More details of these works are available below.

## Progressed tasks in 2021 Research Roadmap:

Research tasks outlined in the 2021 Topic 1 research plan that have been progressed in this round of study are listed below:

- Enhancing IBR response during and subsequent to faults (Urgent topic)
- Developing alternative control methodologies for GFMIs: Inertial response (mimicked SG's inertia) causes post-fault oscillations. APRC, modified q-prioritised-CL, and angle freezing have been proposed and investigated to mitigate the negative impacts of inertial response. In addition, negative sequence current control for GFMIs has also been studied in this round.

The proportion of tasks outlined in the research plan that have been accomplished during the Stage 2 work in the 2022/23 period:

- Enhancing IBR response during and subsequent to faults (Urgent topic) – 40%
- Developing alternative control methodologies for GFMIs – 25%

Table 1. Progress against major tasks listed in the 2021 Roadmap.

| Major task in the 2021 Roadmap | Subtask | Progress |
|---|---|---|
| Enhancing IBR response during and subsequent to faults | IBRs effect on existing protection systems | N/A |
| | Enhancing IBR response during and subsequent to faults |  |
| | Assessment and enhancement of IBRs reliability | N/A |
| | Cyber-secure inverter design for grid-connected applications | N/A |
| Trending Topics | Developing alternative control methodologies for GFMIs |  |
| | Grid-forming capability for HVDC stations and wind and solar farms | N/A |
| | AI in IBRs control | N/A |

# 2. Research completed

## 2.1. Inverter Design Specifications: A review of grid codes and performance standards.

This study, led by the EPRI team and assisted by the Monash team, lays out a set of technical performance specifications aimed at enhancing transmission connected IBR plant's ability to remain connected to the system and support the grid during and subsequent to large signal events (e.g., major system faults, etc.). Additionally, requirements of service provisions, e.g., fast frequency response and negative sequence current, are also summarised in this work.

The approach taken in this study was to review the best and current grid code practices around the world and use some of those requirements to guide inverter performance and design. In addition to that, EPRI team members' practical experience in interconnecting plants in areas of low system strength has also been used to derive some of the performance specifications. Those proven field learnings are useful in the sense that they provide factual proof of inverter features and enable plant interconnection in the field.

This study focuses on the requirements of the FRT capability of IBRs. The required connecting time of IBRs at different levels of fault severity (or no-trip zones) are summarised from various grid codes.

Besides, specifications on active/reactive current, negative-sequence current injection, and response performance of IBRs are reviewed in this investigation.

This study has been drafted in a white paper and published with the final report.

## 2.2. Transient Stability of GFMIs in the Presence of Current Limiters.

Like synchronous generators (SGs), GFMIs are expected to operate as voltage-controlled sources in power systems. They actively try to maintain their point-of-connection (PoC) voltage at a reference value given by higher control layers, e.g., power plant controllers. Thanks to this feature, GFMIs can provide better damping on voltage disturbances and inertial response to quickly tackle frequency disturbances. As a result, in responding to a severe system fault causing a deep voltage sag at the PoC of a GFMI, the GFMI tries to quickly inject an extremely high amount of current into the grid, aiming to recover the PoC voltage. Unlike SGs, which can provide very high overcurrent, a GFMI's offer is limited by thermal capability, thus low overcurrent capability, as the building blocks of GFMIs, similar to any other inverter technology, are semiconductor switches. The overcurrent capability of GFMIs, and inverters in general, is from 1.1 per unit (pu) to 1.4 pu, without oversizing [2]. As a result, during faults and large transient events, a CL engages to protect the semiconductor switches inside GFMIs from the overcurrent. This CL is implemented in the control system of GFMIs.

There are several types of CLs available, including mode switching strategy, magnitude (or circular) limiter, direct (d-) prioritised CL, quadrature (q-) prioritised CL, and virtual-impedance based CL. However, as mentioned in IEEE P2800, IBRs are required to provide the flexibility to set priority to either d- or q- component of the current during faults [3]. Thus, d-prioritised CL (d-CL) and q-prioritised CL (q-CL) are commonly employed. In a conventional cascaded vector control structure, which is built on the dq frame of the PoC voltage of the GFMI, active and reactive currents injected by the GFMI are equivalent to the d- and q- components of the total output current, respectively [4]. In addition, injecting reactive current, or q-current, should be prioritised during faults and voltage sags to support the grid voltage. Hence, q-prioritised CL is focused in this study. More details about this study can be found below.

### 2.2.1. System Configurations of q-prioritised current-limited VSGs

In this study, a single-machine-infinite-bus (SMIB) system consisting of a virtual synchronous generator (VSG), which is a commonly used GFMI type, connected to an infinite bus is considered. The studied system diagram is shown in Figure 1. A simplified diagram of the control structure of the VSG equipped with a q-CL is presented in Figure 2. In this cascaded structure, the primary controller consists of an active power controller (APC) and a reactive power controller. The APC is governed by a virtual swing equation, which is

$$J\frac{d^2\delta}{dt^2} = P_0 - P_{\mathrm{VSG}} - D_{\mathrm{p}}(\omega_{\mathrm{VSG}} - \omega_0), \quad (1)$$

where $P_0$ and $P_{\mathrm{VSG}}$ are the reference and the measured active power of the VSG. $\omega_0$ and $\omega_{\mathrm{VSG}}$ are the nominal and the internal frequencies. $\delta$ is the instantaneous power angle of the VSG with respect to the angle of the infinite bus ($\theta_{\mathrm{g}}$). $J$ and $D_{\mathrm{p}}$ are the inertia and damping coefficients, respectively. The primary control gives references to the voltage controller, which generates references for the inner current loop. The q-CL is inserted between the voltage loop and the current

loop of the VSG. By limiting the current references, the output currents of the VSG can be restrained within the maximum allowable current value, i.e., $I_{\max}$. The q-CL allows the q-current to vary between $-I_{\max}$ and $I_{\max}$, while the remaining amount is allocated to the d-current.

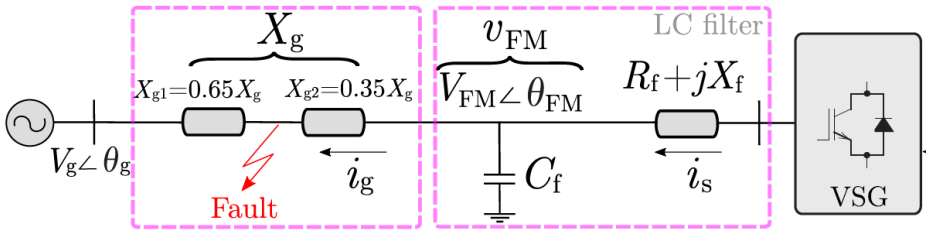


Figure 1. SMIB system.

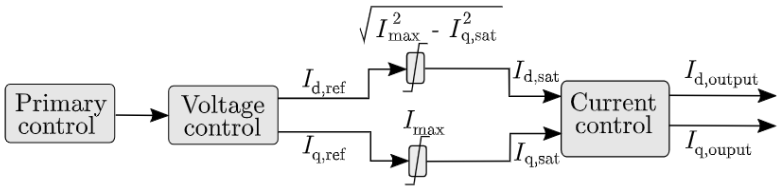


Figure 2. Simplified diagram of the VSG (GFMI) control equiped with a q-CL.

### 2.2.2. Transient Stability Analysis of q-prioritised current-limited VSGs

#### Instability caused by the primary control (APC)

The power-angle curve is a well-known and convenient tool for analysing transient stability and estimating the stability limit of SGs. The power-angle curve of an SG describes the relationship between the active power output of the generator and the angle between the rotor and stator magnetic fields. The active power output of a synchronous generator increases as the angle between the rotor and stator magnetic fields increases until it reaches the maximum value when the angle is at 90 degrees. It then decreases to zero as the angle increases from 90 degrees. The power-angle curve can be employed to study the transient stability of the APC in the primary control shown in Figure 2. Without any CL, the power-angle curve of a VSG is similar to a conventional SG. Unlike an SG, there is no rotating parts, i.e., rotor, in a VSG. Thus, in the power-angle curve of a VSG, the angle δ, generated by (1), replaces the role of the rotor angle in an SG's power-angle curve. An example of the power-angle curve of a VSG without CL is given in Figure 3(a). The movements of the VSG's operating point (OP) on this curve are governed by the swing equation in (1). The unstable equilibrium point (UEP) in this curve can be used as the stability boundary for the VSG. After exceeding the UEP, the VSG enters a positive feedback mode and becomes unstable [5]. In addition, the maximum deceleration area highlighted in Figure 3(a) can serve as an indicator for the stability margin of the VSG. The larger the deceleration area is, the more stable the VSG is, and vice versa.

According to the study we have summarised in [4], when a q-CL engages in the VSG control, the VSG operates as a current-controlled source since the maximum current is reached in this case. This results in a change in the power-angle curve of the VSG. An example of the power-angle curve of a VSG equipped with a q-CL is shown in Figure 3(b). This power angle curve consists of two parts: the voltage-controlled (VC) curve and the current-limited (CL) curve. When the OP reaches the intersection point between these two curves, it transits from one mode to the other. It can be seen

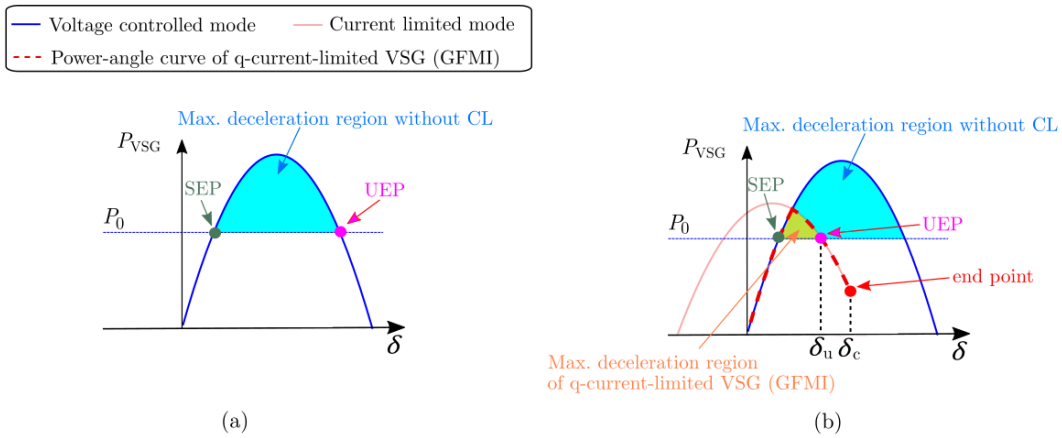


Figure 3. Power-angle curve of (a) VSG without CL and (b) VSG equiped with a q-CL.

from Figure 3 that the UEP of the VSG equipped with a q-CL is much closer to the pre-fault steady-state OP, or the stable equilibrium point (SEP), compared to the case where the CL does not engage. This means that, during and after a large disturbance, the OP is more likely to exceed the UEP if the q-CL engages. Besides, the deceleration area in the case that the q-CL is online is smaller than that in the case without the q-CL. In general, the q-CL deteriorates the stability margin of a VSG.

### Instability caused by the voltage control loop

In addition to the previous analysis, apart from the UEP, in Figure 3(b), there is one more critical point, which is the end point. The analysis, as we summarised in [4], shows that when the OP hits and exceeds the endpoint, the voltage controller shown in Figure 2, starts losing stability due to the disappearance of an SEP in the voltage loop. To understand this type of instability, a criterion for the voltage loop, presented in Figure 4, has been developed and elaborated in [4]. This criterion is similar to the equal-area criterion (EAC).

The criterion for the voltage loop consists of an operating curve, referred to as the $M(I_{\mathrm{q,out}})$ curve, which is a function of the q-current, $\mathrm{I}_{\mathrm{q,out}}$. It is worth noting that the current control is assumed to be ideal as it is very fast compared to the voltage control. Hence, $I_{\mathrm{q,out}}$ approximates $I_{\mathrm{q,ref}}$. The $M$ curve is governed by

$$M(I_{\mathrm{q,out}}) = \sqrt{(I_{\max} X_{\mathrm{g}})^2 - (I_{\mathrm{q,out}} X_{\mathrm{g}})^2}. \quad (2)$$

The quantity $V_g \sin(\delta)$ serves as the reference in this loop. The intersections between the reference and the $M$

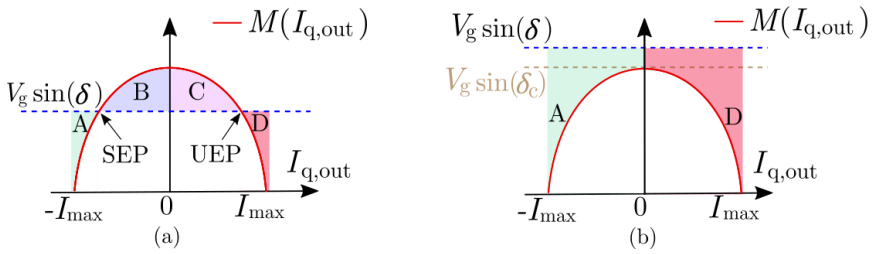


Figure 4. Stability criterion of the voltage loop. (a) with SEP and UEP. (b) no equilibrium point (EP) exists.

curve are the SEP and the UEP of the voltage control loop. Similarly to the EAC and the power-angle curve, there are two unstable scenarios that can occur:

- **Scenario I:** If the OP of the voltage loop exceeds the UEP and enters region D in Figure 4(a), the voltage control loop becomes positive feedback and unstable, leading to the instability of the whole VSG.
- **Scenario II:** If the reference $V_g \sin(\delta)$ does not intersect the *M* curve, there is no equilibrium point. Hence, there is no stable steady state for the voltage control loop to operate in. The voltage control loop and the whole VSG become unstable. This case is represented in Figure 4(b). Unfortunately, during and subsequent to faults, due to the active power imbalance, the angle $\delta$ tends to grow significantly, leading to a relatively high value for the reference $V_g \sin(\delta)$ after a fault clearance. This high value of the reference $V_g \sin(\delta)$ can result in the disappearance of the intersections, i.e., the SEP and UEP. Particularly, in Figure 4(b), if $\delta$ exceeds $\delta_c$, there is no intersections between the reference and the *M* curve. Thus, there is no SEP for the OP of the voltage loop to converge to. The voltage loop becomes unstable eventually as the OP enters region D in Figure 4(b). Therefore, a necessary condition for the voltage control loop and the VSG to remain stable is keeping the angle $\delta$ below $\delta_c$. This $\delta_c$ associates with the endpoint in the power-angle curve shown in Figure 3(b). $\delta_c$ can be calculated as

$$\delta_c = \sin^{-1}\left(\frac{I_{max} X_g}{V_g}\right). \quad (3)$$

Based on the above analysis, the maximum allowable power angle of a VSG equipped with q-CL can be determined as $\min(\delta_c, \delta_u)$, where $\delta_u$ and $\delta_c$ are the angle of the UEP and the end point in Figure 3(b). $\delta_u$ can be identified by solving

$$P_0 = 1.5\, V_g I_{max} \cos(-\delta_u - \phi_{sat}), \text{ where } \phi_{sat} = -\cos^{-1}\left(\frac{V_g \sin\delta_u}{I_{max} X_g}\right)$$

for $\delta_u$ [4].

In other words, the stability limit can be either the UEP or the endpoint in Figure 3(b), depending on their distance to the SEP. The one that is closer to the SEP is the stability limit. This study revisits the transient stability limit of a VSG with a consideration of the q-CL. Based on this study, a more accurate limit for the operating angle of the VSG can be determined.

### 2.2.3. Validations

In this section, three test cases are presented to validate the analysis presented above:

- Case I: This test aims to validate the correctness of the derived power-angle curve of the VSG equipped with q-CL presented in Figure 3(b). Three power-angle curves are analysed in this test: a normal-voltage voltage-controlled (NV-VC) curve, a normal-voltage current-limited (NV-CLd) curve, and a during-fault current-limited (DF-CLd) curve. The NV-VC curve is power-angle curve of the VSG without the CL shown in Figure 3(a). The NV-CLd curve is power-angle curve of the VSG with the q-CL re-activated right after the fault clearance, as shown in Figure 3(b). The DF-CLd curve is power-angle curve of the VSG with the q-CL activated during the fault. The simulated and experimented power-angle trajectories of the VSG are expected to align with these curves during transients. In addition, the stability limit associated with the failure of the primary control (APC) is also validated in this test. It is expected that the VSG will become unstable if the UEP ($\delta_u$) is exceeded.
- Case II: This test aims to validate the stability limit associated with the failure of the voltage control loop. It is expected that the VSG will become unstable if the endpoint ($\delta_c$) is exceeded. This is a validation for scenario II in Section 2.2.2.
- Case III: This test also aims to validate the stability limit associated with the failure of the voltage control loop. It is expected that the VSG will become unstable if the UEP on the *M* curve is exceeded. This is a validation for scenario I in Section 2.2.2. To avoid scenario II from occurring, the APC and the angle $\delta$ are frozen during voltage sags in this test. This assures that $\delta$ always stays below $\delta_c$ in this test.

### Simulations

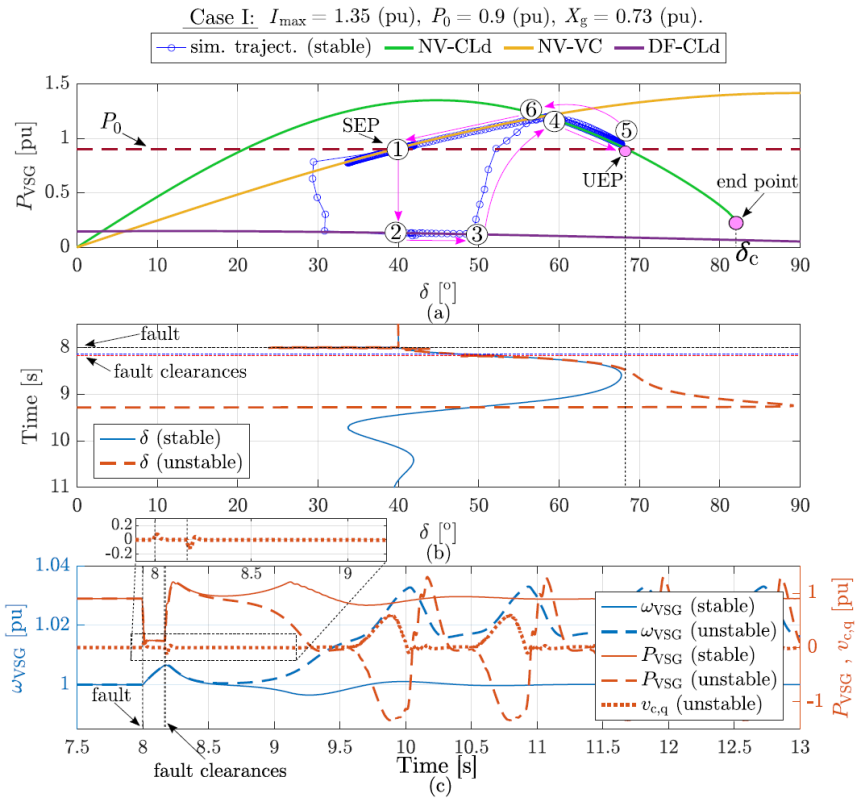


**Figure 5. Simulation validations. Case I: (a) Power-angle curves, (b) time-domain plot of $\delta$, and (c) time-domain plots of active power and frequency.**

The three test cases presented above have been conducted in PSCAD/EMTDC, and their results are summarised in Figure 5, 6, and 7.

In case I, whose results are shown in Figure 5, a fault is applied at t = 8 s and cleared at t = 8.167 s (stable) or t = 8.171 (unstable). In this case, the SEP is closer to the UEP, compared to the endpoint. Hence, the UEP is expected to be the stability limit. In Figure 5(a), the simulated power-angle trajectory of the VSG aligns well with the estimated power-angle curves, i.e., NV-CLd, NV-VC, and DF-CLd, during and after the fault. The fault occurs at point 1, causing a drop of the power to point 2. The trajectory evolves to point 3, where the fault clearance occurs. It then recovers to the NV-CLd curve at point 4. In the stable case, as the trajectory does not exceed the UEP, it is able to exit the current-limited mode at point 6 and converge to the SEP. Whereas, in the unstable case, as $\delta$ grows above the UEP's angle, i.e., $\delta_u$, which is 68 degrees in Case I, the frequency in Figure 5(c) starts reaccelerating at t = 8.6 s. This results in the collapse of the power and the instability of the whole VSG. This test validates the correctness of the estimated power-angle curves and the use of the UEP in the power-angle curve as a stability boundary.

In case II, whose results are presented in Figure 6, there is no intersection between the decreasing side of the NV-CLd curve and the reference power $P_0$. Thus, there is no UEP exists in the primary control of the VSG. Hence, the end point serves as the stability limit in this case. A fault is applied at t = 8 s (point 1) and cleared at t = 8.167 s (point 3). After the fault clearance at point 3, the trajectory moves to point 4 and then approaches point 5. At point 5, the power vertically collapses due to the instability in the voltage control loop. The instability in the voltage control loop can be seen from

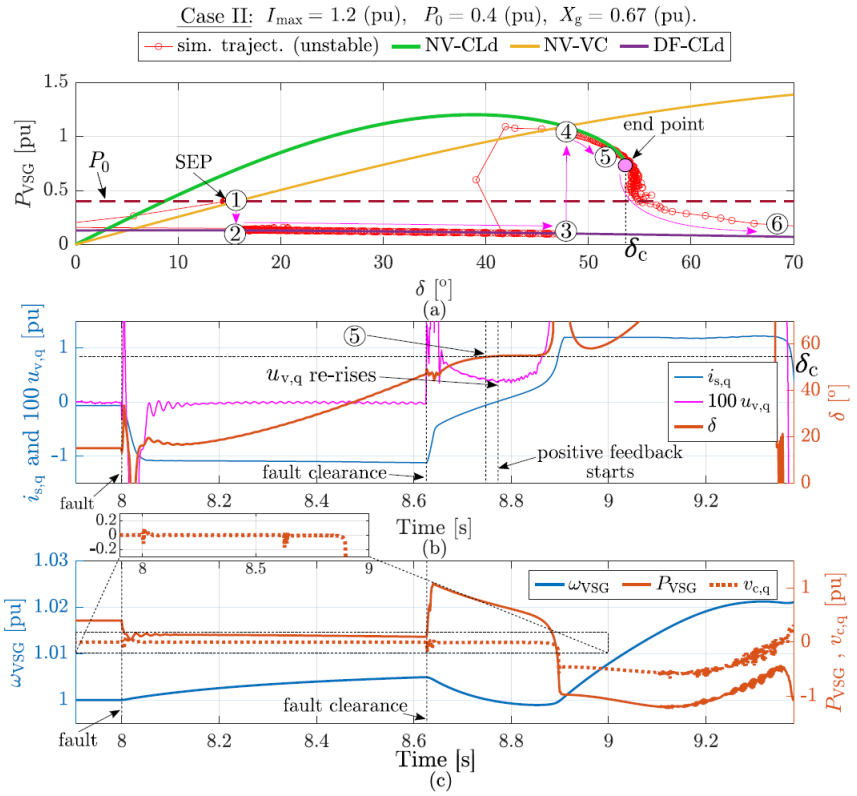


**Figure 6. Simulation validations. Case II: (a) Power-angle curves, (b) time-domain plots of $\delta$, q-current, and (c) time-domain plots of active power and frequency.**

the divergence of the q-current ($i_{s,q}$) to the maximum current value in Figure 6(b). This behaviour validates the use of endpoint as the stability limit in this case.

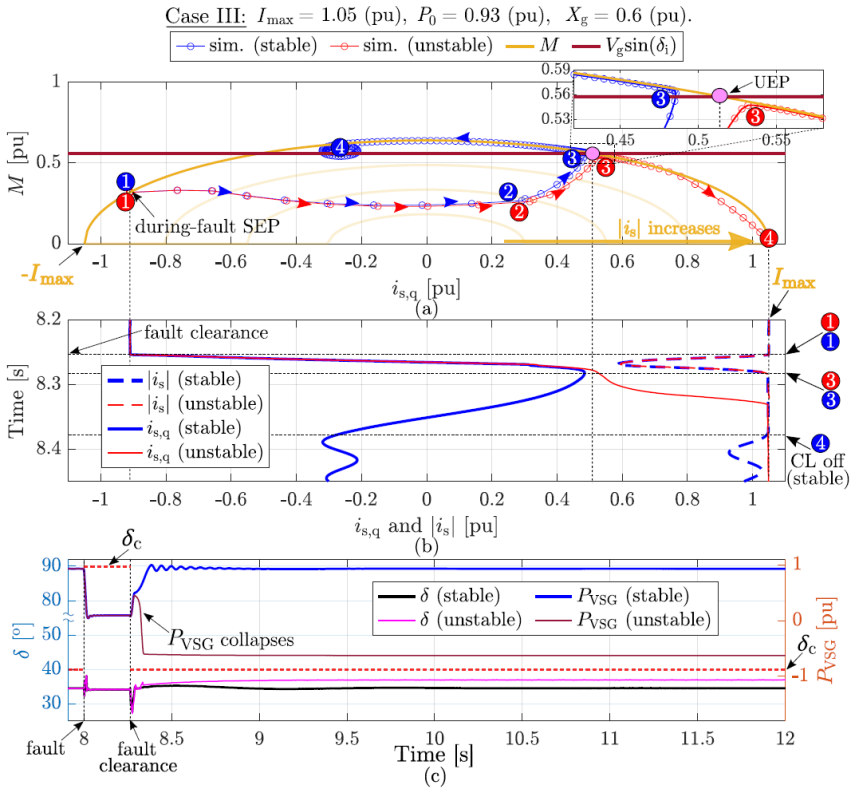


**Figure 7. Simulation validations. Case III: (a) M curves, (b) time-domain plots of q-current and current magnitude, and (c) time-domain plots of active power and $\delta$.**

In case III, whose results are summarised in Figure 7, as the angle is frozen, δ stays around its initial value, which is 34 degrees and remains below $\delta_c$ , as shown in Figure 7(c). The UEP of the voltage control loop is highlighted in Figure 7(a). A fault is applied at t = 8 s and cleared at t = 8.25 s (point 1). The control parameters of the voltage loop are adjusted to create a stable case and an unstable case. As shown in Figure 7(a) and 7(b), and discussed in scenario I of Section 2.2.2, if the trajectory of the OP in the voltage loop exceeds the UEP, the voltage loop becomes unstable due to a positive feedback mode in the voltage control loop. This leads to a rise of the q-current ($i_{s,q}$) to the maximum current value, as shown in Figure 7(a) and 7(b), and a collapse of the active power, as shown in Figure 7(c). This observation validates the criterion developed for scenario I in Section 2.2.2.

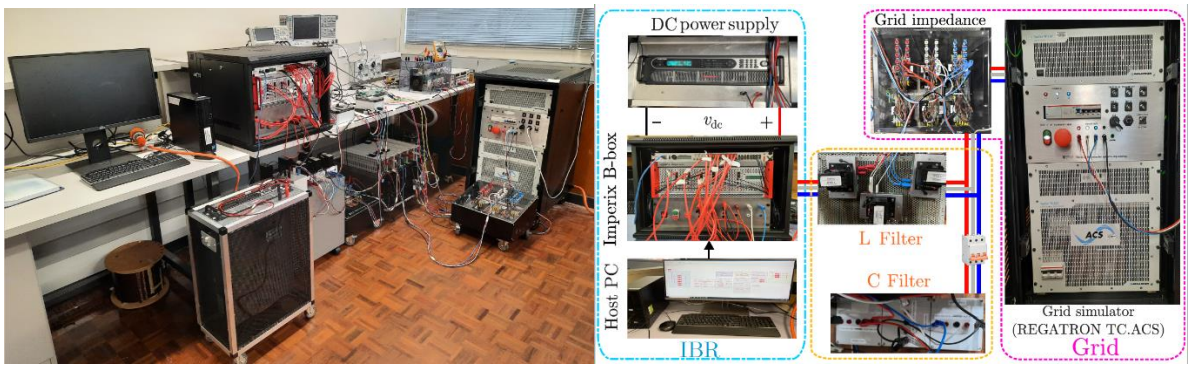


Figure 8. Experimental setup.

The studies above have also been validated in a physical experimental setup at Monash University. The tested system is similar to Figure 1. A photo of the experimental setup and a block diagram made of the photos of the individual components are shown below. The experimental setup is essentially a SMIB system and consists of a 30-kVA Regatron AC power supply emulating a three-phase grid, passive components representing filters and transformers, and an IBR. The IBR, being a three-phase DC/AC converter, is implemented by an Imperix three-phase SiC-based inverter controlled by an Imperix Boombox controller. The IBR is fed by a DC power supply at its DC side.

The three test cases above have been conducted in the experimental testbench. Their results are summarised in Figure 9, 10, and 11. The experimental results are similar to the simulation results and align with the estimated stability boundaries.

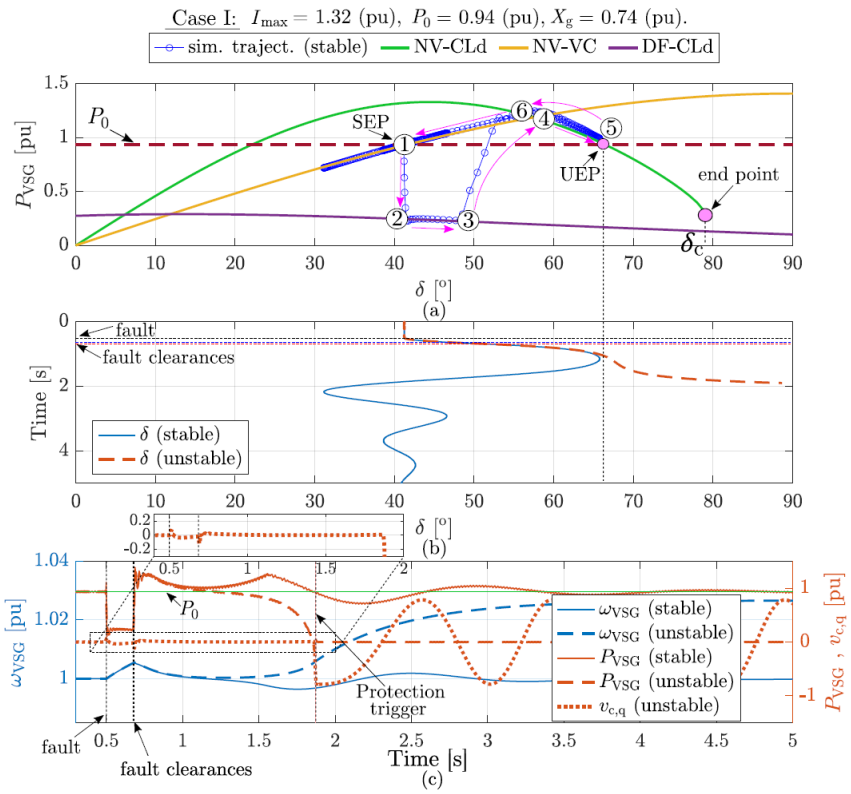


Figure 9. Experimental validations. Case I: (a) Power-angle curves, (b) time-domain plot of $\delta$, and (c) time-domain plots of active power and frequency.

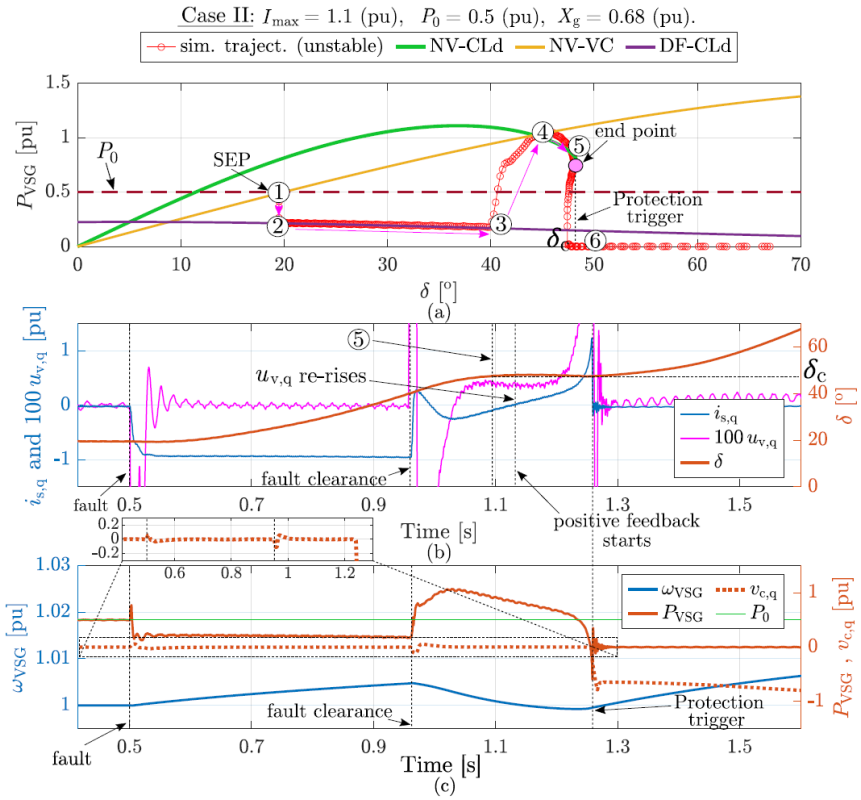


**Figure 10. Experimental validations. Case II: (a) Power-angle curves, (b) time-domain plots of $\delta$, q-current, and (c) time-domain plots of active power and frequency.**

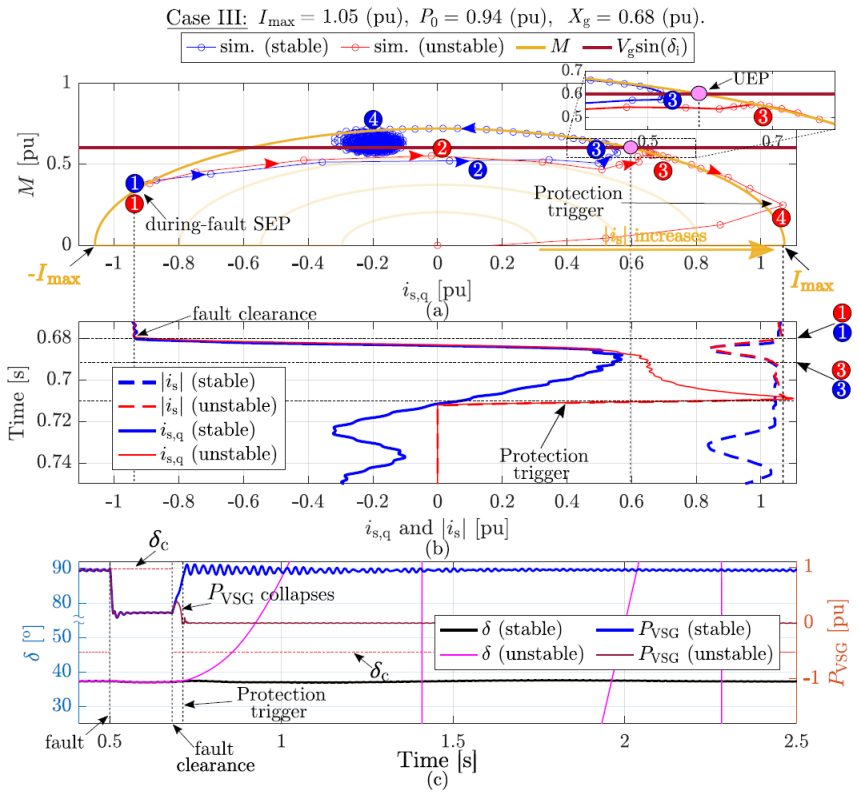


Figure 11. Experimental validations. Case III: (a) M curves, (b) time-domain plots of q-current and current magnitude, and (c) time-domain plots of active power and $\delta$.

### 2.2.4. Applications of the study

Although injecting reactive current during large transients is necessary as discussed in the white paper mentioned in Section 2.1, it is shown in this study that setting priority to reactive current by prioritising q-current of VSGs might exhibit several limitations, apart from benefits. This study identifies a novel angle limit, i.e., $\delta_c$, for q-CL-VSGs, apart from the known UEP angle ($\delta_u$). This limit is caused by the voltage control loop, which is usually overlooked when studying the transient stability of VSGsThis implies a potential degradation of the voltage control stability in the fault recovery process caused by the q-CL. It is recommended to take this limit into consideration when designing and connecting a q-CL-VSG to a PoC in the grid. A sufficient distance between the normal operation of the VSG and this limit should be maintained to ensure its robustness against large transients.

The angle limit $\delta_c$ is determined by (3), where the grid impedance can be estimated by either the worst-case-scenario short-circuit ratio (SCR) at the PoC or an online impedance identification [6]. Based on this limit, the approximate critical clearing time (CCT) of the VSG can be obtained. Therefore, the parameters of the VSG are reviewed and adjusted such that the CCT satisfies no-trip zones specified by grid codes and standards. Several methods, such as backward integral, can be employed to derive the CCT.

Moreover, enhancing controls can be developed based on the analysis presented in this study to either push the limit away from the operating regions the VSG or prevent the OP of the VSG from exceeding the limit. These are continuations of this study.

## 2.3. Transient Stability of Paralleled GFMI-GFLI Systems

As GFLIs, e.g., solar or wind farms, exhibit stability issues in weak areas of the grid, grid-forming battery energy storage systems (GFM-BESSs) are installed in those areas to improve the stability of the local network. Due to the promising application of paralleled GFMI-GFLI systems [7], they are expected to appear more in the near-future power systems. Thus, transient stability analysis of GFMI-GFLI systems is conducted in this project to prepare for the upcoming integrations of such systems.

In this study, the stability boundaries of each IBR and the whole paralleled system are determined and validated. Based on this study, the impacts of different system parameters on the stability of the paralleled system are quantitatively and quickly evaluated. A metric, referred to as deceleration volume (DV), is proposed to measure the reserve deceleration force of the paralleled system. This is a variant of the well-known deceleration area used for assessing the stability of a single machine.

An auxiliary control, referred to as adaptive power reference control (APRC), is also proposed for GFMIs and designed based on the outcomes of the analysis conducted in this study. The APRC helps enhance the transient stability of the paralleled system in various scenarios. More details about the APRC can be found in Section 2.4.

### 2.3.1. System Configurations of paralleled GFMI-GFLI systems

The system diagram of the paralleled GFMI-GFLI (or VSG-GFLI) system is shown in Figure 12. The VSG and the GFLI are connected to a common bus, whose voltage is $V_1\angle 0$. The voltage angles of the VSG and the GFLI are $\delta$ and $\theta$, respectively. The common bus is connected to an infinite bus, which emulates the grid, via a grid impedance as shown in Figure 12. The VSG's synchronisation is governed by a swing equation, eq. (1), while the GFLI synchronises with the grid via a phase-locked loop (PLL) [8]. More details of the internal controls of the VSG and the GFLI are presented in [8].

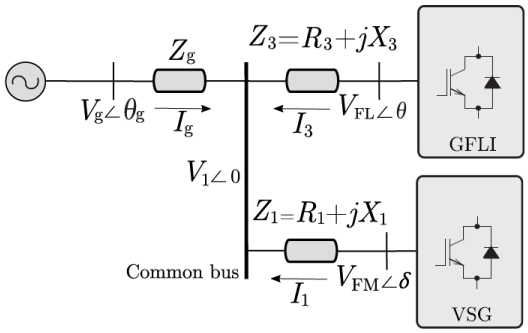


Figure 12. Diagram of the paralleled VSG-GFLI system.

### 2.3.2. Transient Stability Analysis of the VSG-GFLI System

In this paralleled system, the VSG is connected to the GFLI via the common bus. Hence, the common bus is the only coupling point between the two IBRs. Investigating variations of this common bus voltage allows understanding the impacts of one IBR on the other. Therefore, the first step in this

study is deriving a function that captures variations in the common bus voltage $V_1$ with respect to changes in $\delta$ and $\theta$. In other words, a function in the form

$$V_1 = f(\delta, \theta) \tag{4}$$

is obtained to enable analysing the transient stability of the paralleled system. An effort has been made to derive this function. The complete version of this $V_1$ function, which is derived in this project, can be found in [8]. An example of the common bus voltage, i.e., $V_1$, surface is shown in Figure 13. In this figure, the variations of $V_1$ with respect to changes in $\delta$ and $\theta$ are presented. This figure shows the operating domain of the paralleled system.

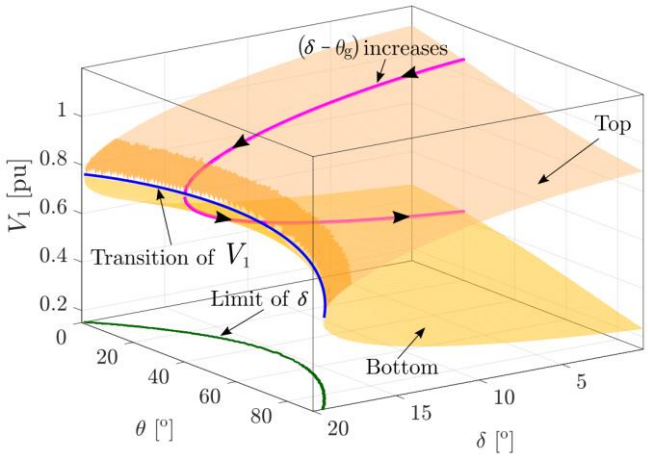


Figure 13. An example of how $V_1$ varies with changes in $\delta$ and $\theta$.

Based on the EAC developed for a single VSG and a GFLI [8], the transient stability of the paralleled system is analysed. In fact, the EAC is only applicable for a SMIB system, e.g., only one IBR and an infinite bus. Thanks to the $V_1$ surface derived above, the EAC can be applied to each IBR in this system separately without losing information about the impacts of the other IBR and the grid. The focus of this work is on the paralleled system. Extensions to a more complex system are within the scope of future works. The conventional EAC is developed for the power-angle curve of an IBR. To extend this method to the paralleled system, the EAC is modified to analyse the system in a voltage-angle space. This modification results in two critical voltage surfaces, which are $V_{\mathrm{c,VSG}}$ and $V_{\mathrm{c,GFLI}}$ presented in Figure 14(a) and (b). The derivations of $V_{\mathrm{c,VSG}}$ and $V_{\mathrm{c,GFLI}}$ are available in [8]. When $V_1 < V_{\mathrm{c,VSG}}$, the frequency of the VSG increases, and if $V_1 > V_{\mathrm{c,VSG}}$, the frequency of the VSG reduces. It is worth noting that at an EP, $V_1 = V_{\mathrm{c,VSG}}$. Thus, the intersections between $V_1$ and $V_{\mathrm{c,VSG}}$, i.e., Line I and Line II, represent the sets of the stable EP (SEP) and the unstable EP (UEP) of the system. The exact locations of the SEP and the UEP are the intersections between these lines and the $V_{\mathrm{c,GFLI}}$ surface. Line I is where the SEP belongs to as the voltage of this line is around 1 pu.

The $V_{\mathrm{c,VSG}}$ divides the $V_1$ surface into acceleration regions, i.e., A and D, and deceleration regions, i.e., B and C. If the OP of the system enters region D after a fault clearance, the power angle control of the VSG becomes positive feedback. This results in a divergence of the OP from the SEP, which is located on Line I. Similarly, the acceleration and deceleration regions of the GFLI can also be obtained by analysing the intersections between the $V_1$ surface and the $V_{\mathrm{c,GFLI}}$ surface.

Therefore, the intersections between $V_{\mathrm{c,VSG}}$ and $V_1$ help identify the stability boundaries and the set of equilibrium points of the VSG. Similarly, the intersections between $V_{\mathrm{c,GFLI}}$ and $V_1$ play the same

role for the GFLI. In Figure 14(c), the stable and unstable operating region of the paralleled system are presented. Line II and Line b can serve as the stability boundaries for the paralleled system. If the OP of the paralleled system always stays in the stable region, the operation of the paralleled system can converge to a stable steady-state. In addition, the SEP and UEP of the paralleled system can be identified in this voltage-angle analysis, as shown in Figure 14(c). A 2-D top view of the voltage-angle space is included in Figure 14(d) for better visualisation.

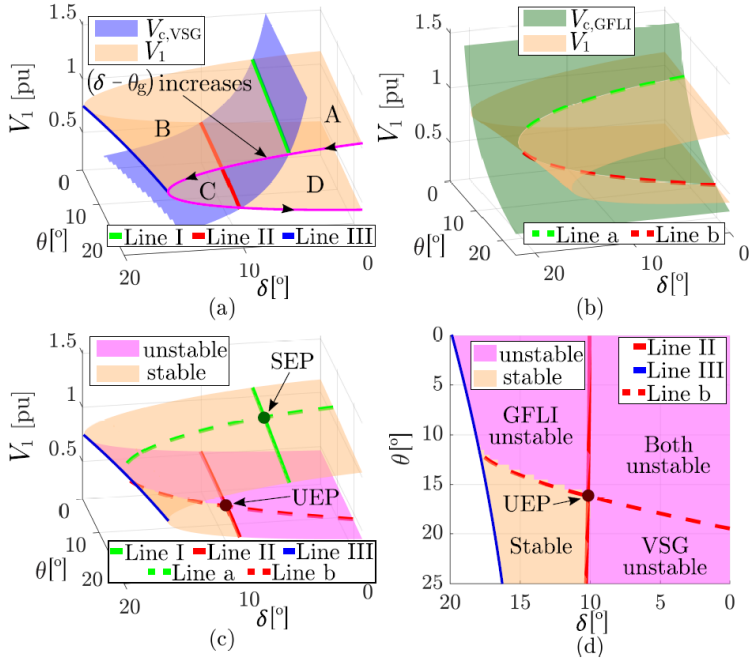


**Figure 14. An example of how the stability boundaries are determined: (a) Stability boundary of the VSG, (b) Stability boundary of the GFLI, (c) Stability boundaries of the VSG-GFLI system, and (d) 2-D top view of the stability boundaries**

The distance between the SEP and the UEP in Figure 14(c) can indicate how stable the system is. The longer this distance is, the more stable the system is. Moreover, another index has been proposed in this study to quantify the stability margin of the paralleled system. It is referred to as deceleration volume (DV). The DV is an extension of the deceleration area developed from the conventional EAC. It represents how much reserve deceleration force available in the paralleled system. Thus, a system with a larger DV has a larger transient stability margin. The DV is the volume

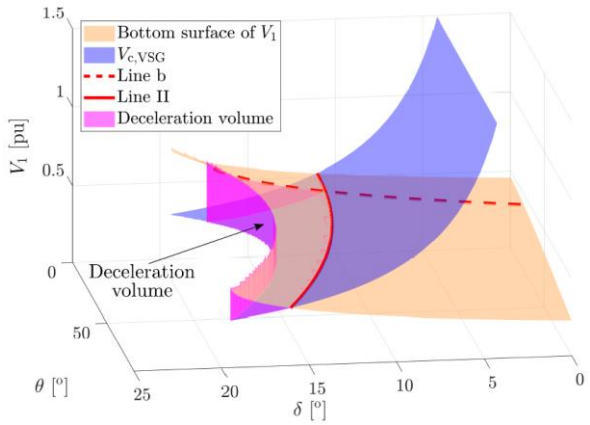


**Figure 15. Deceleration volume presentation**

highlighted in Figure 15. More details on this analysis are available in [8].

### 2.3.3. Validations

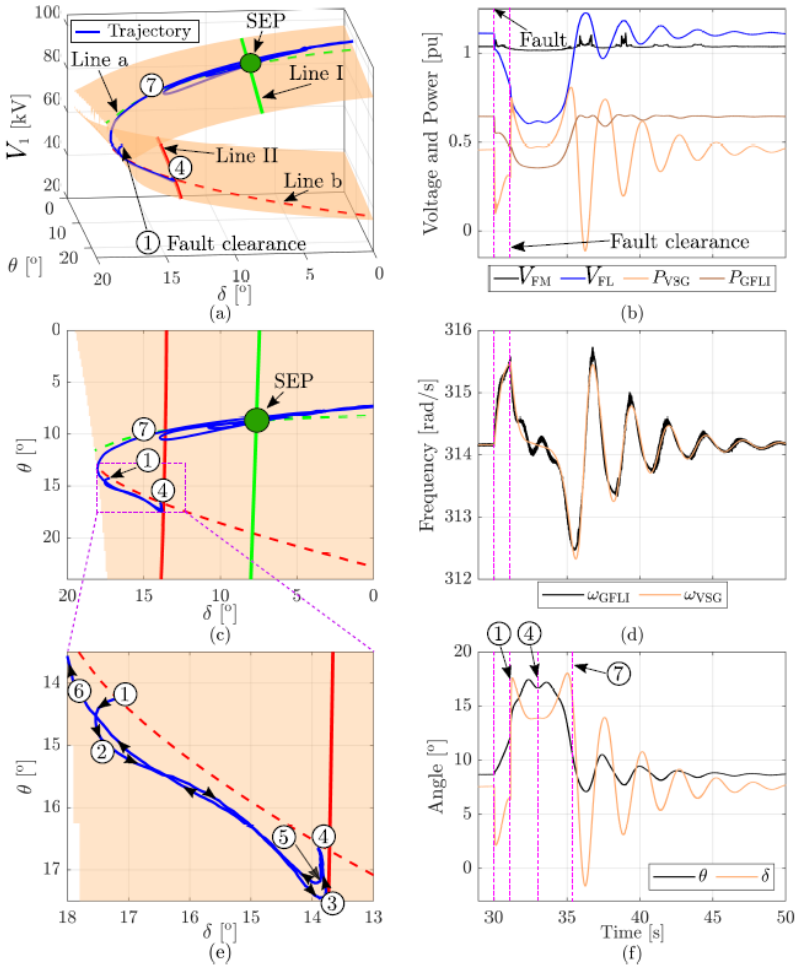


**Figure 16. Simulated responses of the system to a voltage sag when the system is marginally stable: (a) 3-D view of the angle trajectory, (b) Time-domain voltage and active power, (c) 2-D top view of the angle trajectory, (d) Time domain frequency, (e) Magnified 2-D top view of the angle trajectory, and (f) Time-domain angles.**

Time-domain simulations have been conducted to validate the stability boundaries presented above. A voltage sag is applied at t = 30 s. A marginally stable case is obtained by clearing the fault at t = 31.123 s. The results of this case are summarised in Figure 16. The fault clearance occurs at point 1 of the trajectory. The inertia of the VSG pushes the trajectory toward the stability boundary of the VSG (line II). As the trajectory still does not cross line II, it is then able to return to the SEP. The paralleled system remains stable in this case.

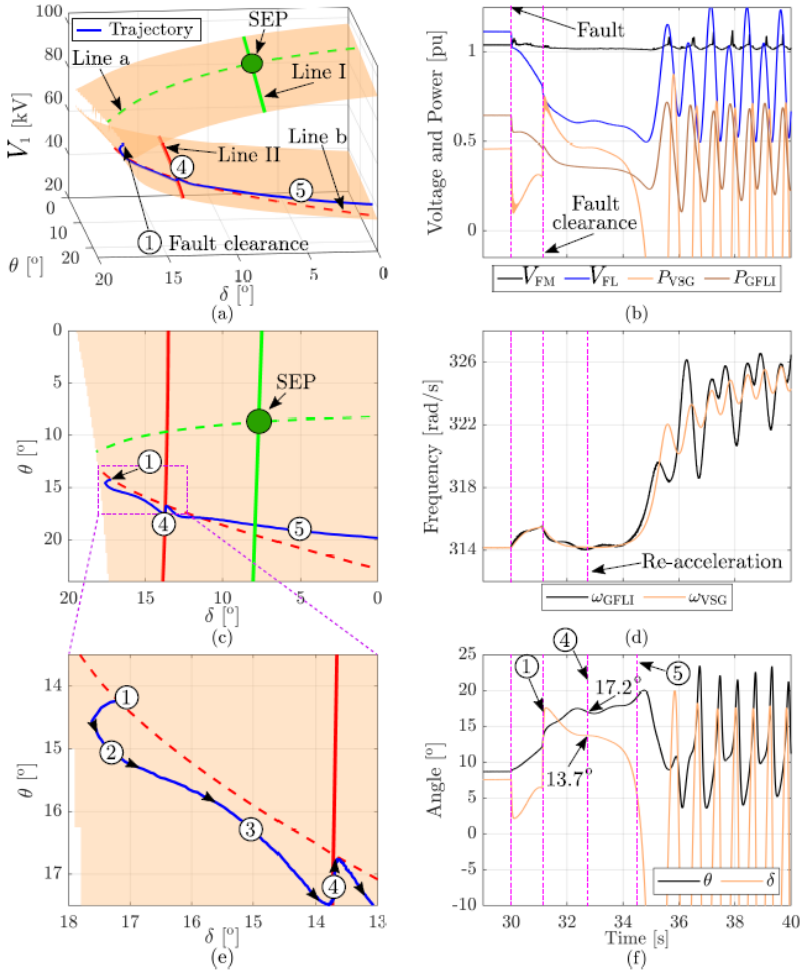


**Figure 17. Simulated responses of the system to a voltage sag when the system becomes unstable: (a) 3-D view of the angle trajectory, (b) Time-domain voltage and active power, (c) 2-D top view of the angle trajectory, (d) Time-domain frequency, (e) Magnified 2-D top view of the angle trajectory, and (f) Time-domain angles.**

The fault clearance instant is increased to t = 31.1235 s to make the system unstable. The results of this case are summarised in Figure 17. In this case, the trajectory crosses the stability of the VSG (line II) and enters the unstable region at point 4. At the crossing instant (point 4), the frequencies in the system start re-accelerating as shown in Figure 17(d). The system then becomes unstable. Moreover, at the crossing instant (point 4), the angles δ and θ are 13.7 degrees and 17.2 degrees, respectively. These values match the crossing location (point 4) in the trajectory plot (Figure 17(e)). Hence, this validates the correctness of the stability boundary.

The two test cases above were also replicated in an experimental testbench consisting of a paralleled VSG-GFLI system. The results of the stable and unstable cases are presented in Figure 18. The correctness of the stability boundary is again validated in the experiment testbench.

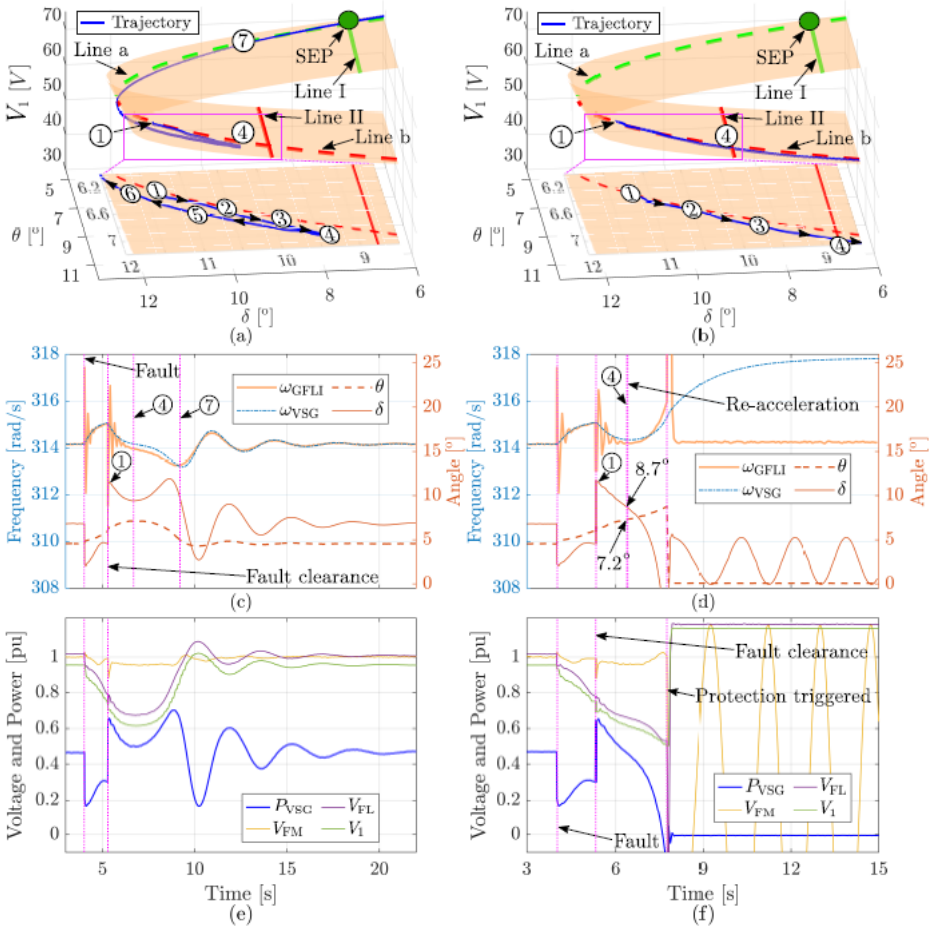


Figure 18. Experimental validation of the stability boundaries of the paralleled system. Stable case: (a) angle trajectory, (c) frequency and angle, (e) voltage and power measurements. Unstable case: (b) angle trajectory, (d) frequency and angle, (f) voltage and power measurements.

### 2.3.4. Applications of the study

This study can be applied to understand how stable a GFMI-GFLI system is, when designing the GFMI-GFLI system. The stability boundaries and the DV introduced above can be used as stability indicators for the system. Demonstrations of the stability boundaries are available in section 2.3.3 and Sections III-C and III-D of [8]. The system in these examples remains stable if its operating point stays in the identified stable region, while it becomes unstable when the operating point enters an unstable region. The analysis presented in Figure 14 shows how far the pre-fault operating point, i.e. SEP, of the system is, from the stability boundaries, i.e., Line II and Line b. Based on this indicator, system parameters can be adjusted to maximise the stability margin of the system, by bringing the pre-fault operating point away from the stability boundaries. For example, an increase in $Z_g$ makes Line II closer to Line III and the SEP in Figure 14. Based on the above analysis, other parameters, such as the dispatch levels of the IBRs, can be adjusted to regain the same distance between Line II and the SEP as before the growth of $Z_g$. In addition, the operational limits of the paralleled system can be determined from the studies presented in this work.

## 2.4. Transient Stability Enhancing Methods and Negative Sequence Current Injection for GFMIs

### 2.4.1. Adaptive Power Reference Control (APRC)

An additional angle droop controller, referred to as APRC, is proposed to improve the transient stability of the paralleled VSG-GFLI system discussed in Section 2.3. During voltage sags, the APRC adjusts the active power reference, i.e., $P_0$, of the VSG based on an adaptive controller shown in Figure 19. It helps the paralleled system recover to a stable operation faster. In general, the APRC improves the damping of the active power control loop of the GFMI to mitigate post-fault power swings. Based on the analysis in Section 2.3, the APRC can be tuned and designed such that the operating point (OP) of the whole paralleled system can remain in a stable operation. If the fault is

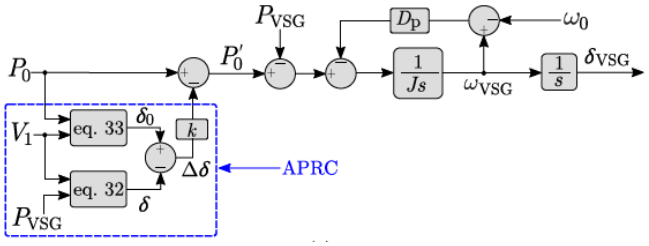


Figure 19. Diagram of the APRC. Note: eq. 32 and eq. 33 in this figure refer to the equations in [8].

not severe and the system can stably converge to the pre-fault dispatch, the APRC allows the operating point to follow the pre-fault dispatch levels. Whereas, if the fault is too severe for the dispatch levels to be met, the APRC adaptively reduces $P_0$ to create a new SEP for the operating point to stably converge to.

From Figure 19, the APRC is added to the swing equation of the VSG as an add-on. This controller estimates the angle difference between the real-time power angle of the VSG and the angle value that it should converge to, i.e., $\Delta\delta$. This angle difference represents how far $\delta$ should travel to get $P_{\text{VSG}}$ equal to $P_0$, and is used to adjust the power reference of the VSG. It is worth noting that eq. 32 and eq. 33 in Figure 19 refer to the equations in [8], not in this report. It is shown in [8] that the APRC acts as a variable power-frequency droop gain. When the common bus voltage $V_1$ drops deeply due to a fault in the system, the APRC reduces the overall droop gain of the power-frequency control to help the VSG remain stable. However, this behaviour can affect the power sharing of the VSG in a steady state. Thus, the APRC is only active when the PoC voltage falls below a certain value, e.g., 0.85 pu.

It is also shown in [8] that the APRC improves the damping of APC of the VSG. Moreover, if the fault is too severe for an SEP of the paralleled system to exist, the APRC adjusts the power reference in a way such that a new SEP is created for the OP of the system to converge to. Besides, the APRC is designed to maintain the steady-state common bus voltage $V_1$ above a given threshold value. The threshold value for $V_1$ can be selected from the analysis presented in Section 2.3. By this approach, the stability of the GFLI is also maintained.

The performance of the APRC has been evaluated in the experimental testbench at Monash University. Two test cases have been conducted: one with an SEP existing during a voltage sag and one without any SEP existing. In Figure 20(a) and (b), without the APRC, the system becomes

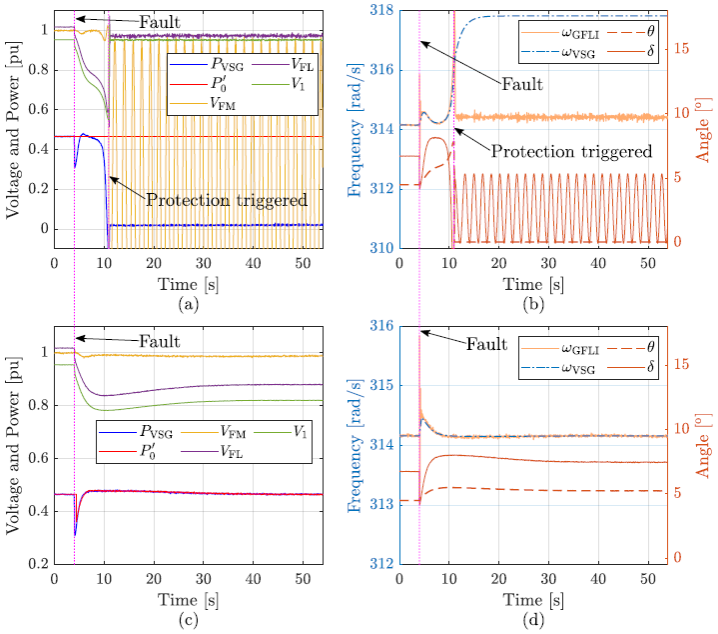


**Figure 20. Experimental validation of the APRC with an SEP existing during a voltage sag. Without the APRC: (a) voltage and power, (b) frequency and angle measurements. With the APRC: (c) voltage and power, (d) frequency and angle measurements.**

unstable shortly after the occurrence of a voltage sag of 0.8 pu at t = 4 s due to a lack of damping in the VSG control. Voltages and powers collapse while the frequencies diverge from their nominal value in this case. On the other hand, with the APRC active, more damping is provided. The paralleled system can remain stable without much transient. As there is an SEP existing in this case, the VSG power, i.e., $P_{\mathrm{VSG}}$, can converge to its pre-fault reference value as shown in Figure 20(c). This shows that as long as the paralleled system is able to remain stable, the VSG can stick to the power command without decreasing the injected power unnecessarily. In an overload event where the voltage sag is not too severe, if the VSG cuts down generations immediately, the power imbalance becomes worse and might lead to the instability of the system. Thus, the APRC is designed to avoid that undesired scenario.

To further validate the enhancements brought by the APRC, a test case without any SEP during a voltage sag has been conducted. The voltage sag is set to 0.6 pu and occurs at t = 4 s in this case. The results of this case are presented in Figure 21. Without the APRC, the system becomes unstable due to the absence of an SEP during the voltage sag as presented in Figure 21(a) and (b). When the APRC engages, as in Figure 21(c) and (d), it reduces the power reference, $P_0$, to stabilise the system. The powers and voltages converge to a stable steady state in this case. The fault clearance is not included in this case to validate the performance of the APRC in a harsh condition.

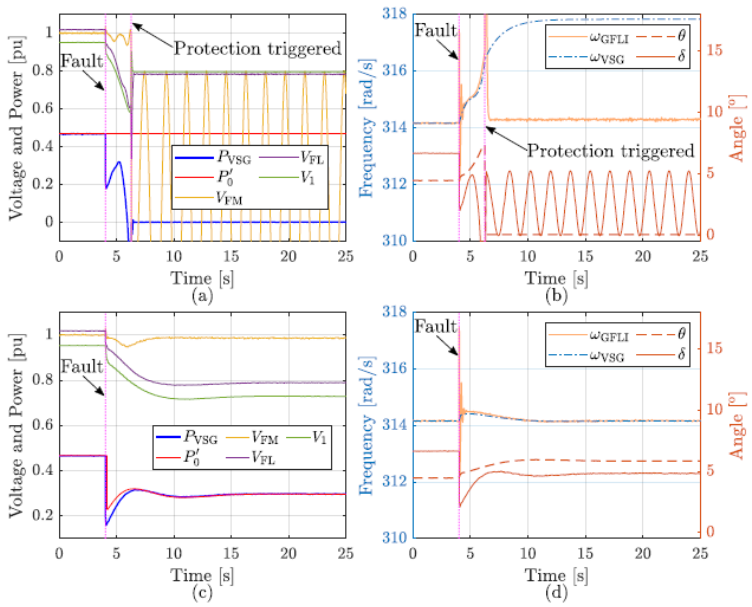


Figure 21. Experimental validation of the APRC without any SEP existing during a voltage sag. Without the APRC: (a) voltage and power, (b) frequency and angle measurements. With the APRC: (c) voltage and power, (d) frequency and angle measurements.

### 2.4.2. Modified q-Prioritised Current Limiter

This is a modification of the q-prioritised current limiter (q-CL) discussed in Section 2.2. This modification helps keep the GFMI stable, even when the novel stability limit caused by the violation of the stability criterion of the voltage control loop discussed in Section 2.2 is exceeded.

The conventional q-CL sets the operating range of the q-current to $[-I_{\max},\ I_{\max}]$. However, as shown in Figure 4, the positive feedback region, which is the unstable region denoted as D, is located on the positive side of the q-current ($I_{q,out} > 0$). During voltage sags, e.g., PoC voltage is below 0.9 pu, if the operating range of the q-current is set to $[-I_{\max},\ 0]$, the OP of the voltage control loop will not enter region D. Hence, instability caused by the positive feedback mode of the voltage control loop is avoided. This modification of the q-CL will be tested in the functionality tests presented in Section 2.6.

### 2.4.3. Freezing Active Power Control Loop During Faults

In synchronous generators (SGs), the swing equation is almost a fixed physical characteristic. The angle growth, caused by a power imbalance on the input of the swing equation during faults, leads to the risk of instability and prolonged recoveries. On the other hand, the synchronisation of a virtual-synchronous-generator (VSG-)based GFMI, is governed by a virtual swing equation implemented in its control software. Thus, it is more flexible to integrate an auxiliary control to mitigate the undesired behaviours caused by the angle growth. To avoid the angle growth caused by a power imbalance that SGs experience, in VSG-based GFMIs, the active power imbalance is frozen when a fault is detected. This keeps the OP of the GFMI close to the pre-fault location, hence resulting in less severe post-fault transients.

### 2.4.4. Negative Sequence Current Injection from GFMIs

As conventional synchronous generators are displaced, their contributions to fault levels and sequence profiles are also reduced in many areas. IBRs will not inherently provide negative sequence current contributions unless the controls are designed to either inject or suppress negative sequence current. However, for the existing protection architecture to remain effective, IBR plants are required to inject negative sequence currents during fault conditions to help increase the level of unbalanced currents in the network during unbalanced fault conditions. In this regard, grid codes and standards have started to provide the minimum requirement for negative sequence current injection during unbalanced fault conditions.

IEEE Std. P2800 [3] requires IBRs to inject negative sequence current (dependent on the unit negative sequence voltage) in addition to the injection of positive sequence current. The negative sequence current shall meet the following condition:

- leads the unit's negative sequence voltage by 90 to 100 degrees for full converter-based IBRs and 90 to 150 degrees for type III WTGs

However, similarly to the requirement for positive sequence current, the standard does not state a specific magnitude for the negative sequence current but provides the minimum requirements as below:

- IBR shall be capable of injecting a negative sequence reactive current of 50% of its maximum current rating when the IBR unit terminal negative sequence voltage becomes greater or equal to 25% of the nominal voltage
- Injection of a higher negative sequence reactive current for a lower negative sequence terminal voltage is permitted

Additionally, if the IBR's total current limit is reached, the standard state that either the positive or negative reactive current injection or both may be reduced, but preference is given to reducing both currents. However, the incremental reduction in the positive sequence reactive current should not be higher than that in the negative sequence reactive current. The proportion of how much positive and negative sequence current must be provided is currently the subject of research.

Similarly, German Grid Code (VDE-AR-N 4120 Technical Connection Rules) [9] also requires the injection of negative sequence reactive current based on a specific characteristic curve. The amount of negative sequence current injection is proportional to the negative sequence voltage by factor "k," which is defined as the characteristic proportional gain and can take a value between 2 and 6.

A model of a GFMI with negative sequence current controls is developed to assess the impact of including these controls on the behaviour of these units during unbalanced faults. The following general recommendations were considered when designing the negative sequence controls:

- During unbalanced faults, IBRs should be able to inject negative sequence reactive current up to a limit of 50% of its current capacity, depending on the amount of the terminal negative sequence voltage.
- If the IBR's total current limit is reached, either the positive or negative or both can be reduced; however, the reduction in the positive sequence reactive current should be equal to or smaller than the reduction in the negative sequence reactive current.

- The proportion of how much positive and negative sequence current must be provided is currently the subject of research.
- The design parameters for the negative sequence reactive current injection can be taken from the German Grid Code
- A defined ratio between positive and negative sequence is not prescribed as a one-size-fits-all ratio may not be suitable. The type of unbalanced conditions that may occur makes it hard to specify a single ratio of positive and negative current contributions. Anecdotal evidence from some grid authorities that are implementing negative sequence contribution requirements indicates that, in many cases, performance is agreed to on a case-by-case basis between the plant and the grid authority. Some grid authorities have also refrained from requiring specific ratios of negative sequence contribution as it could lead to excessively high voltages on non-faulted phases, possibly causing unintended plant tripping or other issues associated with high transient voltages. Therefore, this guide will refrain from prescribing a specific ratio between positive and negative sequence current contributions as more research and practical evidence are needed on this topic.

#### 2.4.4.1 Negative Sequence Current Controller:

The negative sequence controls in the GFM model are implemented to meet the basic requirements of IEEE P2800 and German grid code in terms of negative sequence current injections, which means:

- Priority is given to reactive current in both positive and negative sequence
- No injection of negative sequence current during normal operation
- Injection of negative sequence current based on the negative sequence voltage at the inverter terminal with current leading the voltage by 90° to 100°.

Figure 22 shows the block diagram of the negative sequence current controller. During asymmetrical grid faults, when there exists a non-zero negative sequence component of grid voltage, the inverter is designed to inject a certain amount of negative sequence current. For this purpose, the negative sequence voltage components, $\boldsymbol{vd}_2$, and $\boldsymbol{vq}_2$ are extracted using the Dual Decoupled Synchronous Reference Frame (DDSRF) method [10], and the magnitude of negative sequence voltage is used as the input signal to a gain block, Kqv2. Setting Kqv2 = 0 disables the negative sequence voltage control, and the inverter regulates the negative sequence current to zero. For the assessments performed in this section, Kqv2 is set to 3 and 5. To ensure the injection of negative sequence reactive current that leads to the negative sequence voltage component, 90 degrees is subtracted from the voltage phase angle. Additionally, a dead-band can be designed according to the requirements of protection systems to allow the injection of negative sequence current only when negative sequence voltage increases beyond a specific limit.

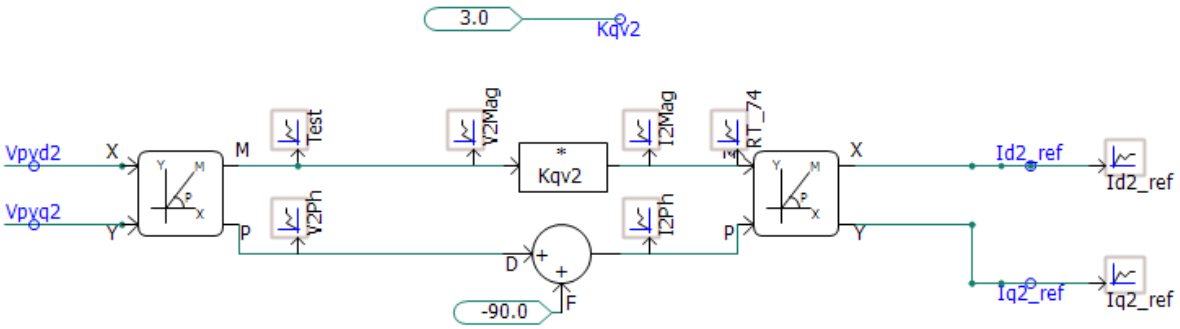


Figure 22. Negative Sequence Voltage Controller

**Current Limit Logic:**

The current references developed by the outer control loop are limited to ensure the resulting phase currents of the inverter do not exceed the specified current limit. If the current references result in the inverter current exceeding the limit in at least one of the phases, the current limit logic prioritises components of the current based on the following:

- The reactive current is prioritised over the active current.
- More priority is given to the positive sequence current over the negative sequence current (this is a modification to the original negative sequence model to help synchronise with the grid via the power-synchronising mechanism of GFMIs (VSG control)).

The current limits logic of the model used in this section is implemented in two steps [11] [12]:

- **Step 1:** Step 1 of the current limit logic is implemented by comparing the maximum value of the space vector of the current in $\boldsymbol{\alpha\beta}$ frame ($\boldsymbol{i_{\alpha\beta}}$) to the inverter's current limit. The maximum value of the space vector of the current is considered to be the addition of the magnitude of the positive and negative sequence components (an assumption that the two vectors are aligned).

  The positive sequence current has the highest priority in the logic. If the current limit is exceeded in any phase, the magnitude of the negative sequence current is scaled down using a scale factor called "*scale*" to gain more room for the positive sequence current.

$$\text{scale} = \frac{I_{\text{lim}}}{I_{\text{phase,max}}}, \tag{5}$$

  where $I_{\text{phase,max}}$ is the highest phase current that exceeds the current limit, i.e., $I_{\text{lim}}$. On the other hand, if the maximum phase current does not exceed the current limit, there is no need to scale down the current limit of the negative-sequence current, and there might be capacity for injection of the full amount of negative sequence current determined by the control in Figure 22. The positive sequence q-current magnitude is allowed to grow up to $I_{\text{lim}}$-$\left|i'_{d2} + ji'_{q2}\right|$, where $\left|i'_{d2} + ji'_{q2}\right|$ is the magnitude of the scaled negative sequence current. If the current does not reach its limit, the remaining room is assigned to positive d-current, i.e., $i_{\text{d1}}$. Thus, $i_{\text{d1}}$will be limited to:

$$i_{d1lim} = \sqrt{\left(I_{lim} - \left|i'_{d2} + ji'_{q2}\right|\right)^2 - i'^2_{q1}}, \tag{6}$$

where $i'_{q1}$ is the positive sequence q-current. By this arrangement, the priority is set to the positive sequence q-current, hence the positive sequence reactive current as presented in Section 2.2.

- **Step 2:** The logic explained in Step 1 is based on using the maximum value of the space vector of the current, which may overestimate the maximum phase current depending on the phase difference between the positive and negative sequence currents.
  Obtaining the phasor currents based on the symmetrical components of current and solving for the magnitude of each phasor current, a second scaling factor can be defined in the second step of current limit logic to maximize the phase currents.

$$Scale_{Max} = \frac{\boldsymbol{I_{lim}}}{\boldsymbol{max}(|\boldsymbol{I_a}|+|\boldsymbol{I_b}|+|\boldsymbol{I_c}|)} \quad (7)$$

The simulation performed here uses the total current capacity in Step 1, so Step 2 logic is not included.

#### 2.4.4.2 Performance Evaluations

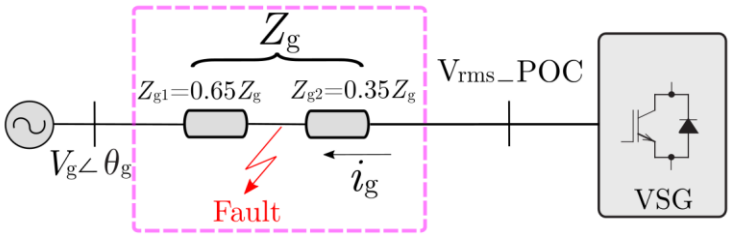


Figure 23. Test system of the negative sequence current control

The investigated system is shown in Figure 23. A VSG equipped with the negative sequence (NS) current control presented above is tested in various conditions listed in Table 2. The base voltage and base power are 138 kV and 100 MVA. The current limit, i.e., $I_{\text{lim}}$, is set to 1.5 pu. The grid impedance $Z_g$ is kept at 0.15 pu.

Table 2. Simulation parameters of the negative sequence current control tests

| Case | Number of faulty phases | Power dispatch (pu) | Reference voltage (pu) | Fault duration (ms) | Angle freezing | Kqv2 | Result |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0.6 | 1.05 | 2000 | Off | 0 | Figure 24 |
| 2 | 1 | 0.6 | 1.05 | 2000 | Off | 3 | Figure 25 |
| 3 | 2 | 0.6 | 1.05 | 450 | Off | 0 | Figure 26 |
| 4 | 2 | 0.6 | 1.05 | 450 | Off | 3 | Figure 27 |
| 5 | 2 | 0.65 | 1.05 | 450 | Off | 3 | Figure 28 |
| 6 | 2 | 0.65 | 1.05 | 450 | Off | 5 | Figure 29 |
| 7 | 2 | 0.65 | 1.05 | 450 | On | 5 | Figure 30 |

For each tested case,

- NS voltage at the terminal of the VSG,
- active and reactive powers ($P_{VSG}$ and $Q_{VSG}$),

- positive sequence active current ($I_{1,\mathrm{P}}$), positive sequence reactive current ($I_{1,\mathrm{Q}}$), negative sequence active current ($I_{2,\mathrm{P}}$), negative sequence reactive current ($I_{2,\mathrm{Q}}$),
- magnitudes of positive and negative sequence current ($I_{mag,1}$ and $I_{mag,2}$),
- internal VSG frequency,
- grid voltage and current ($V_{grid}$ and $I_{\mathrm{grid}}$)

are presented in Figures 24-30.

**Case 1&2:** In Case 1 and Case 2, whose results are shown in Figures 24 and 25 respectively, a single-phase-to-ground fault is applied to the system. When the NS current control is enabled, as in Case 2, a decent amount of NS current is injected to the system, while the injected current in Case 1 consists of purely positive sequence current as the NS current control is disabled. It is worth noting that there is a voltage swell during the fault when the NS current control is inactive, i.e., in Case 1. Additionally, in Case 2, a phase current reaches the current limit, i.e., 1.5 pu. Thus, the NS current is scaled down, as mentioned above, to give priority to the positive sequence current, as voltage support and synchronisation are more critical to the stability of the VSG. In fact, without the current limiter, the NS current is supposed to grow to 0.54 pu as Kqv2 = 3.

Moreover, the NS current in Case 2, shown in Figure 25, is purely reactive as $I_{2,\mathrm{P}}$ is kept at zero during and after the fault. The NS current instantly drops to zero when the unbalanced fault is cleared. Thus, the NS current control functionality operates properly, as discussed above.

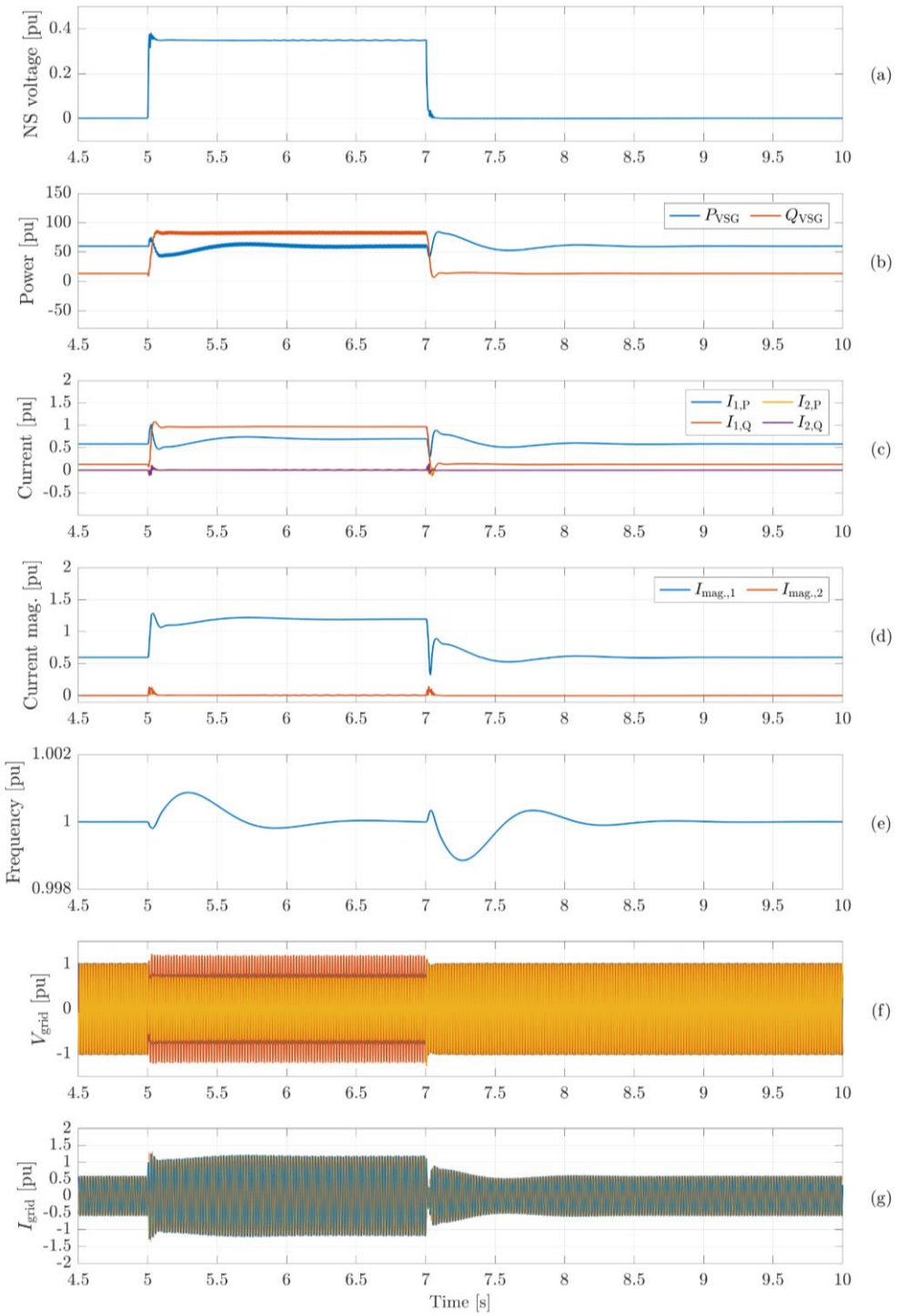


**Figure 24. Simulation results of NS current control. Case 1: (a) NS voltage, (b) Power, (c) current components, (d) current magnitudes, (e) frequency, (f) grid voltage, and (g) grid current.**

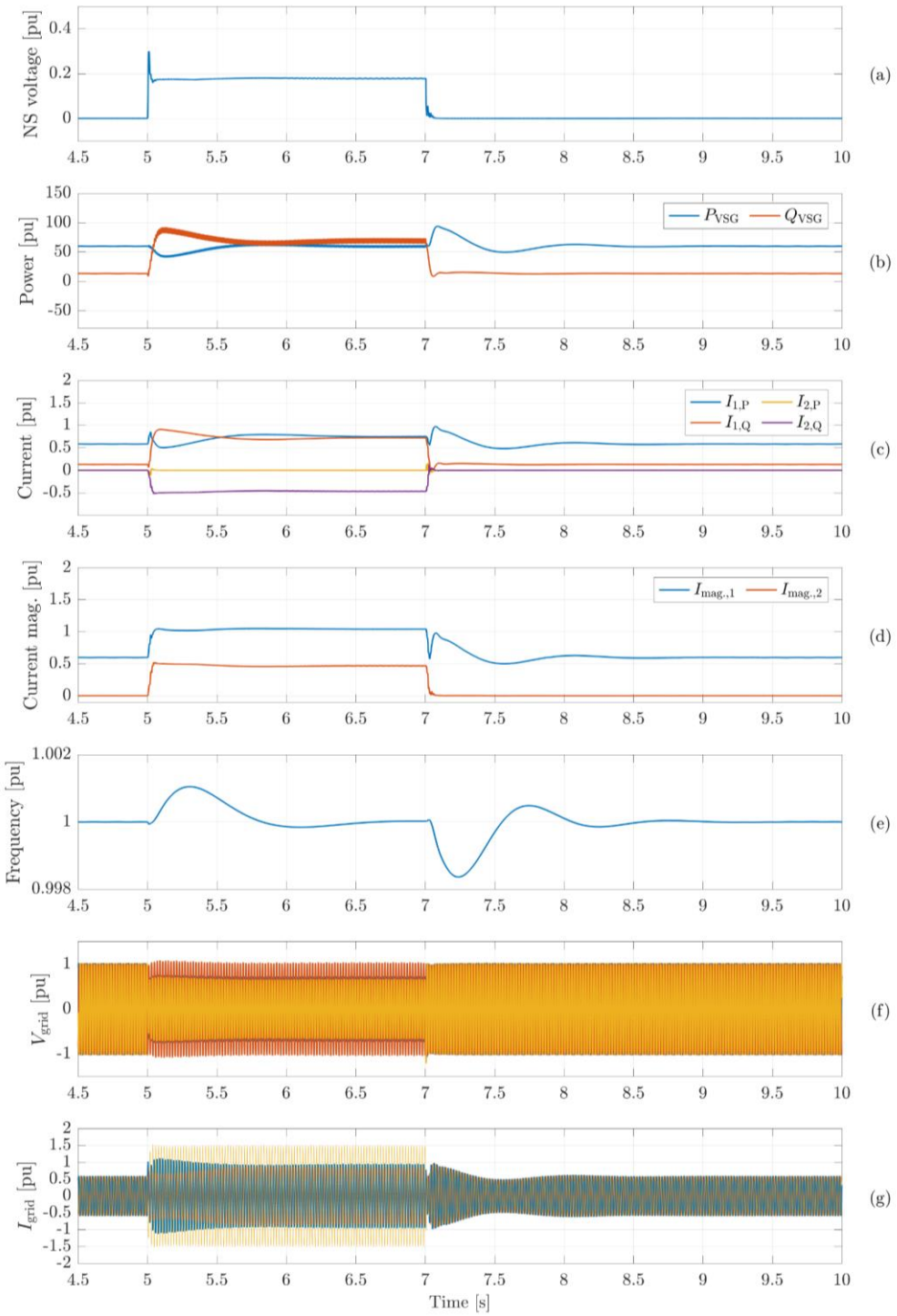


**Figure 25. Simulation results of NS current control. Case 2: (a) NS voltage, (b) Power, (c) current components, (d) current magnitudes, (e) frequency, (f) grid voltage, and (g) grid current.**

**Case 3&4:** In Case 3 and Case 4, whose results are shown in Figures 26 and 27, respectively, a two-phase-to-ground fault is applied. Similarly, in Case 4, the NS current control injects NS reactive current to the grid, while the current in Case 3 is combined purely from positive sequence components. As the fault is more severe compared to those in Cases 1 and 2, a higher positive sequence current is required for synchronising with the grid. Thus, the NS current is scaled down even lower in Case 4, compared to Case 2.

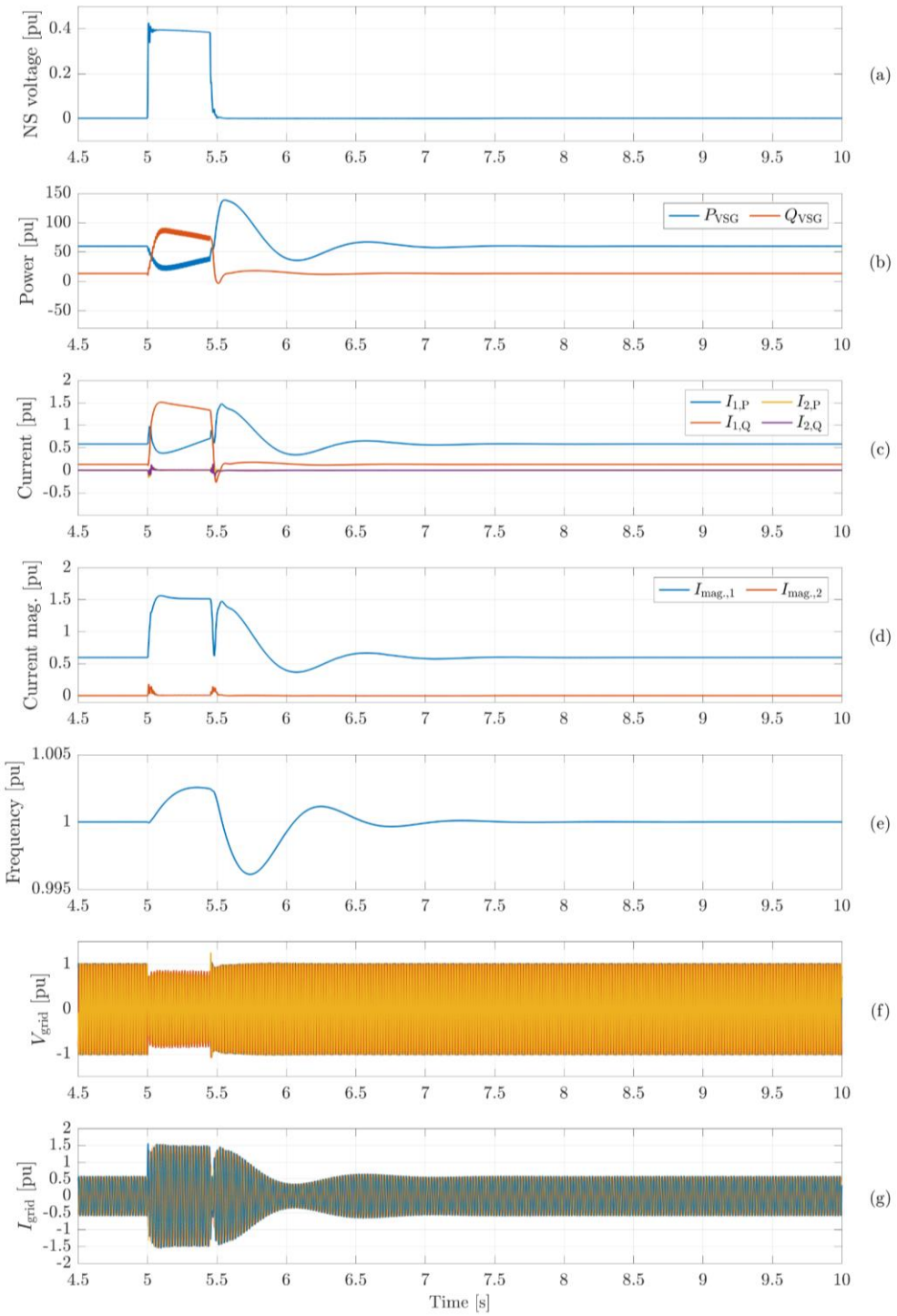


**Figure 26. Simulation results of NS current control. Case 3: (a) NS voltage, (b) Power, (c) current components, (d) current magnitudes, (e) frequency, (f) grid voltage, and (g) grid current.**

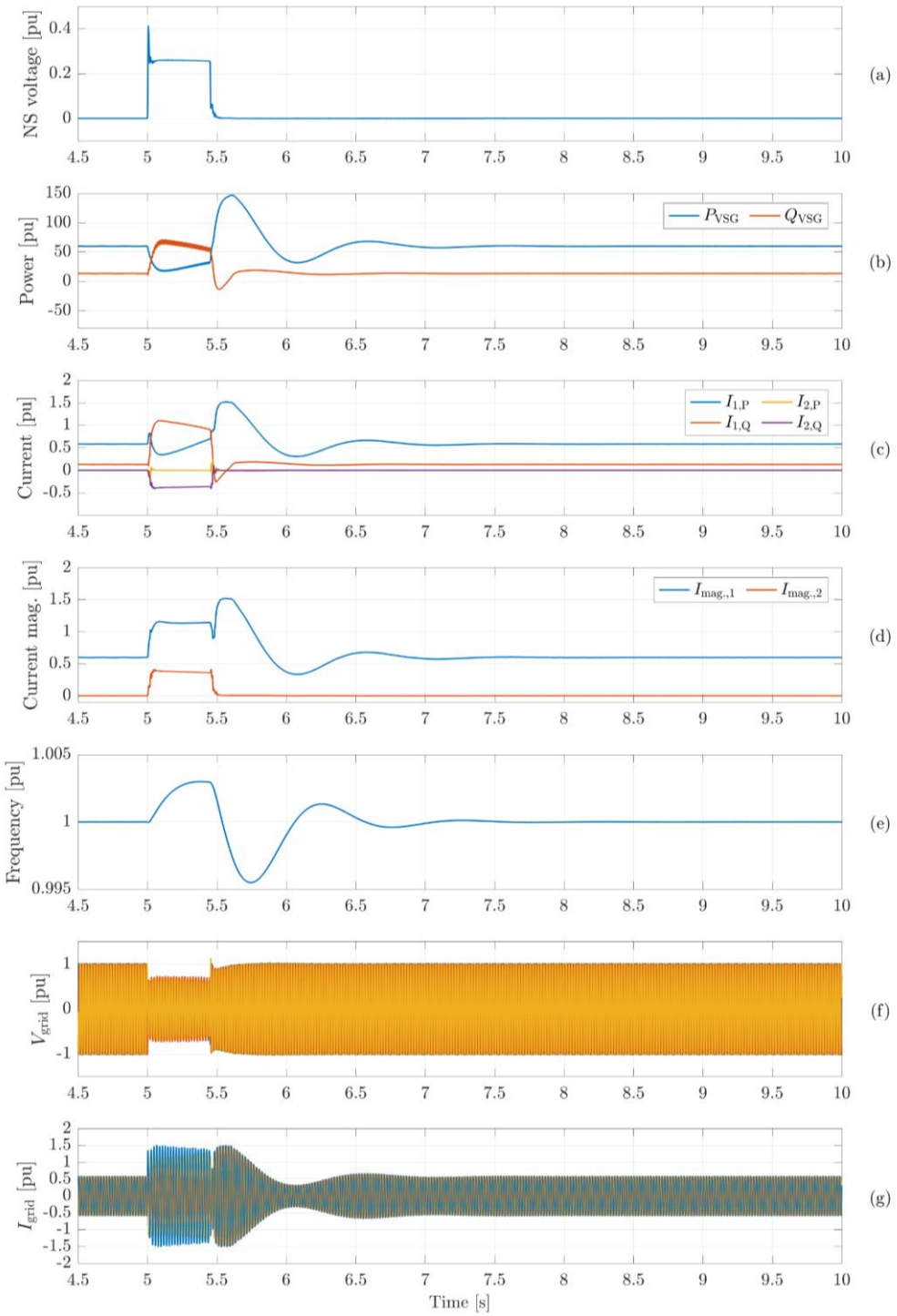


**Figure 27. Simulation results of NS current control. Case 4: (a) NS voltage, (b) Power, (c) current components, (d) current magnitudes, (e) frequency, (f) grid voltage, and (g) grid current.**

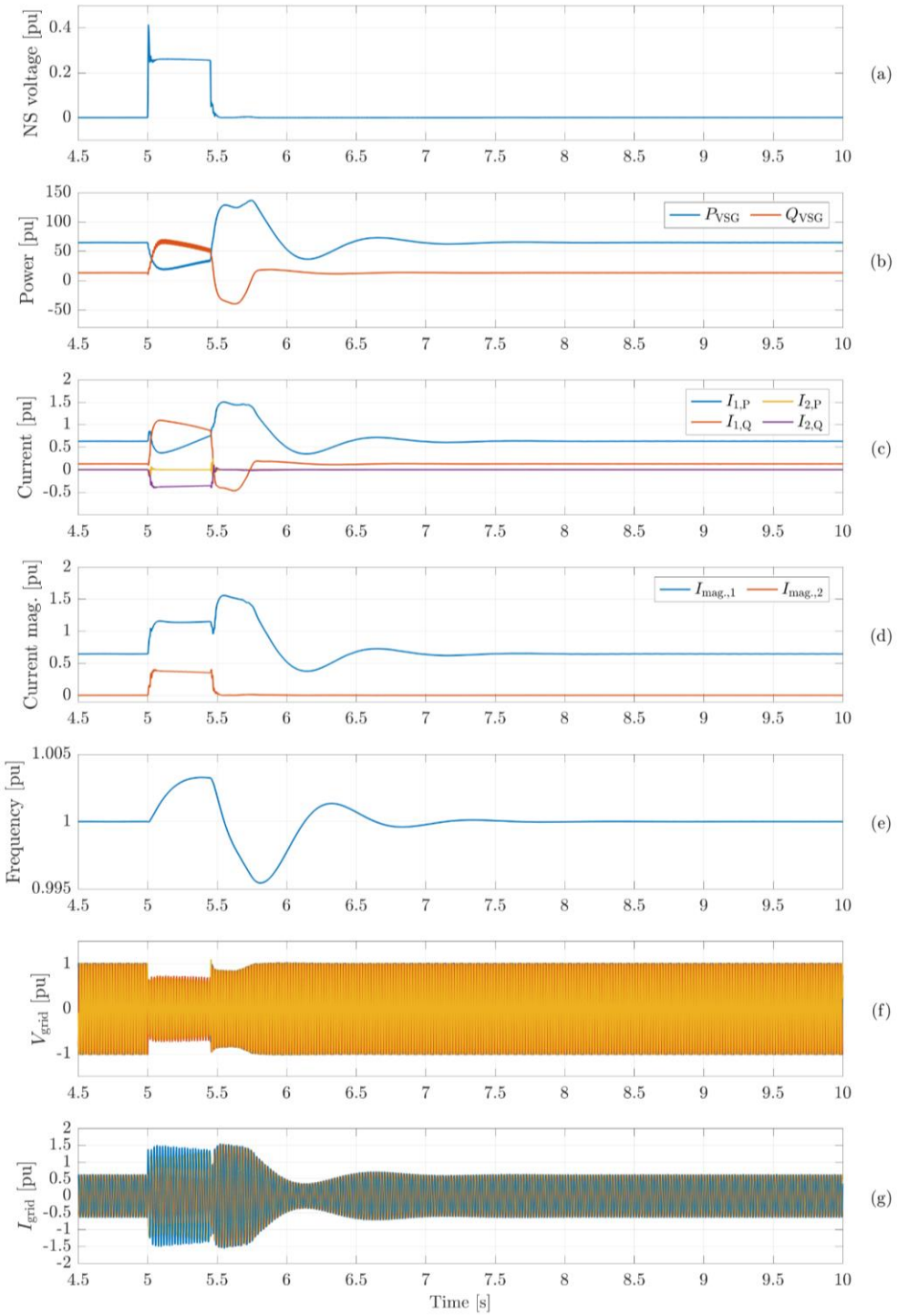


**Figure 28. Simulation results of NS current control. Case 5: (a) NS voltage, (b) Power, (c) current components, (d) current magnitudes, (e) frequency, (f) grid voltage, and (g) grid current.**

**Case 5&6:** In Case 5 and Case 6, whose results are shown in Figures 28 and 29, respectively, a two-phase-to-ground fault is also applied to the system. However, in this case, the power dispatch is increased to 65 MW. Both cases are equipped with the NS current control. However, the gain Kqv2 is set lower in Case 5 (Kqv2 = 3), compared to that in Case 6 (Kqv2=5). The case with the higher gain fails to synchronise with the grid and becomes unstable after the fault clearance. Since the higher Kqv2 tends to inject more NS current, the limit on the positive sequence current component is lower in Case 6. Hence, as discussed in Section 2.2, lower current limits negatively impact the

synchronising loop of the VSG. Therefore, the gain Kqv2 must be carefully designed to reserve sufficient positive sequence current for the synchronisation of the VSG.

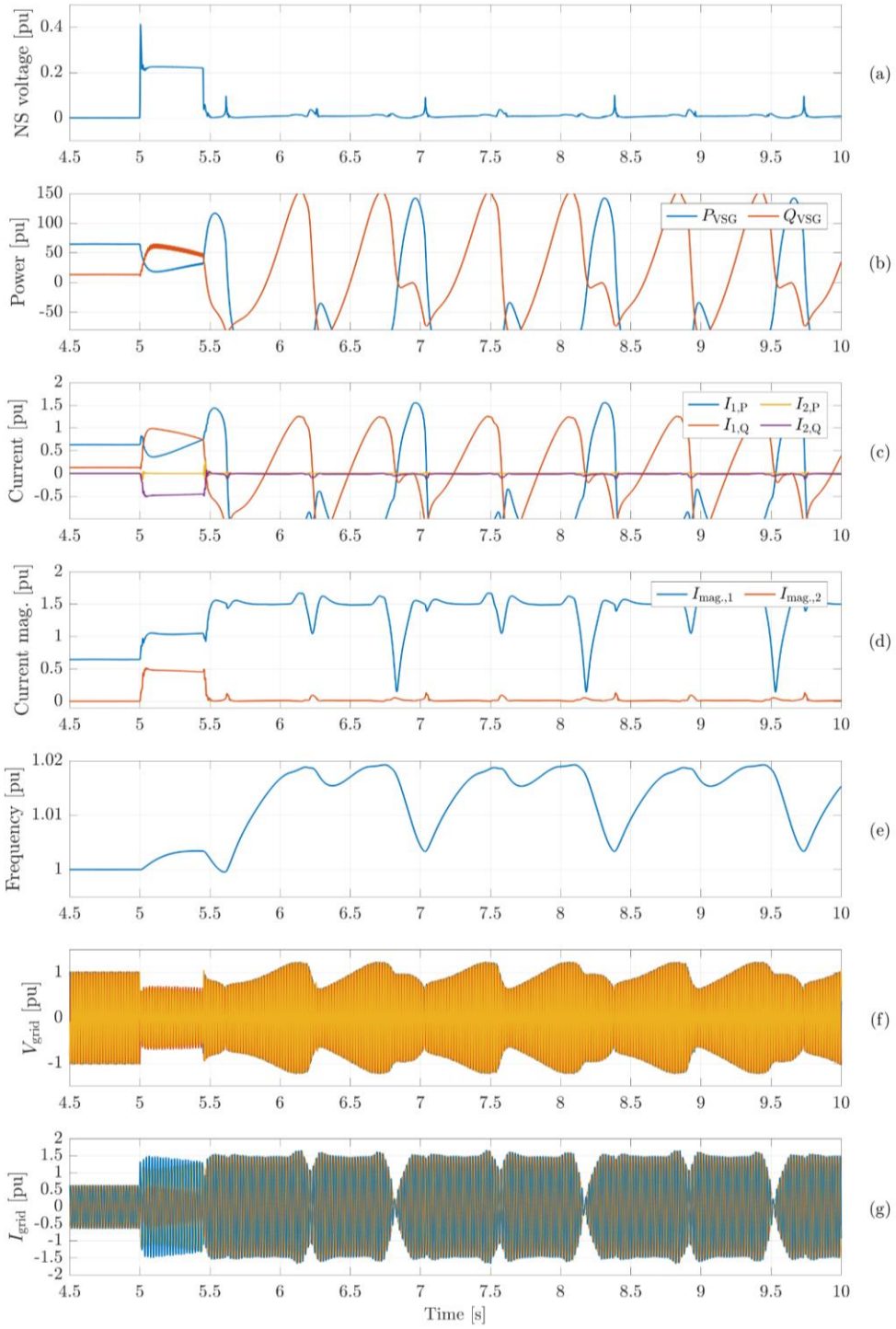


**Figure 29. Simulation results of NS current control. Case 6: (a) NS voltage, (b) Power, (c) current components, (d) current magnitudes, (e) frequency, (f) grid voltage, and (g) grid current.**

**Case 7:** The unstable scenario in Case 6 is repeated with the angle freezing scheme enabled in Case 7. The angle freezing scheme blocks the power error fed to the synchronising loop of the VSG, thus, preventing the power angle growth of the VSG. Therefore, the VSG is stabilised in this case while injecting a higher amount of NS current to the grid compared to Case 5.

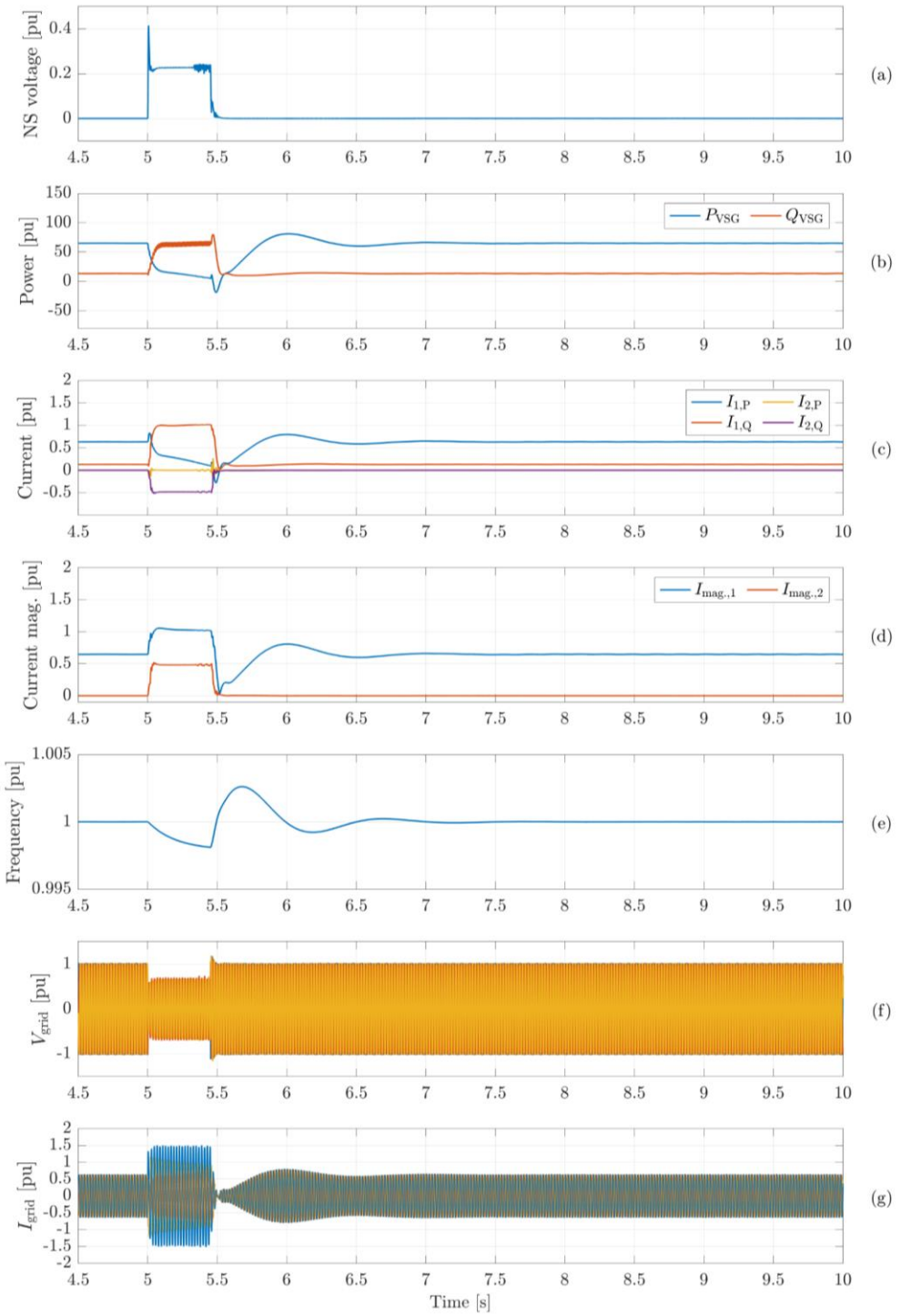


**Figure 30. Simulation results of NS current control. Case 7: (a) NS voltage, (b) Power, (c) current components, (d) current magnitudes, (e) frequency, (f) grid voltage, and (g) grid current.**

### 2.4.4.3 Summary

The NS current control for GFMIs developed and studied in this study injects NS reactive current to unbalanced faults based on the magnitude of the NS voltage at the terminal of the VSG. It is found in this study that with a limited overcurrent capacity of GFMI (or VSG), injecting a high amount of NS current pushes the positive sequence current lower. This negatively affects the transient stability of the synchronising loop of VSGs, as they are power-synchronising based. More studies on

improving the NS control of GFMIs as well as reviewing the protection system's settings are within the scope of future work of this study.

## 2.5. Transient Stability Analysis for Multi-IBR Systems

This study aims to develop indices or indicators to allow quickly measuring the transient stability margin of a system consisting of multiple IBRs. This study can be built on the lessons learned and the analyses conducted for a single current-limited GFMI (Section 2.2) and a paralleled system (Section 2.3).

The synchronising loop of an IBR, i.e., active power control loop for GFMI and phase-locked loop (PLL) for GFLI, has two equilibrium points, i.e., a stable equilibrium point (SEP) and an unstable equilibrium point (UEP). Two examples of the distance between the SEP and UEP of a SMIB system and a paralleled system are shown in Figure 31 with light-blue arrows. If the OP of an IBR exceeds the UEP, the synchronising loop becomes positive feedback, and the OP slides away from the SEP [5]. This results in extremely severe transients in the power and frequency of the IBR. Moreover, the UEP of a paralleled GFMI-GFLI system can be identified as in [8]. The further the SEP is away from the UEP, the further the initial OP is away from a positive-feedback mode; hence the more stable the OP of the system is.

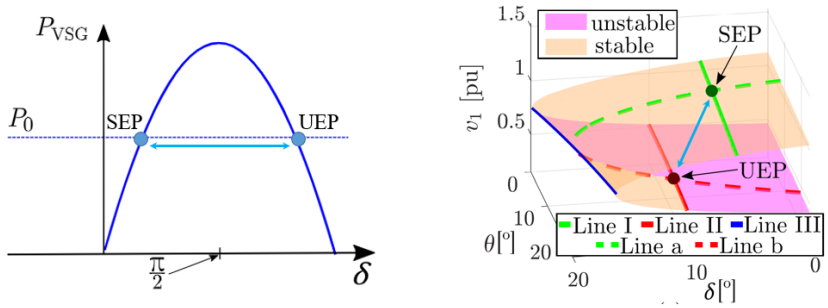


Figure 31. Distance between SEP and UEP in a SMIB and a paralleled system.

The goal of this study is to develop a method/process to quickly measure the distance between the SEP and the UEP of a multi-IBR system in its operating domain. For a SMIB system and a paralleled system, the operating domains are 2-D (the power-angle curve) and 3-D (the voltage-angle space). However, for a system consisting of more than two IBRs, more than three dimensions are required to interpret the operating domain, as each IBR contributes its operating angle as one dimension to the domain. Hence, graphical visualisation may not be applicable. Thus, in this study, instead of exploring the whole operating domain of the multi-IBR system, only the SEP and the UEP are estimated. Once the SEP and the UEP are identified, the distance between them can be calculated to extract a meaningful quantity that represents how far the SEP is away from the UEP. It is worth noting that the SEP and UEP mentioned above are the equilibrium points in the power-angle control loop (the synchronising loop).

In this study, q-CLs, which are investigated in Section 2.2, are employed to protect the IBRs from overcurrents during large transients. Nevertheless, as shown in Section 2.2, when a q-CL is utilised, there exists a possibility that the GFMI/VSG fails due to the instability of the voltage loop before the UEP in the synchronising loop is reached. Hence, there are cases in which no global UEP exists. In

these cases, instead of measuring the distance between the SEP and the UEP of the multi-IBR system, the distance between the SEP and the point where the voltage loop of an IBR starts becoming unstable is estimated and used as the stability margin indicator.

### 2.5.1. System Configurations of the multi-IBR system

Within the context of this research stage, a system consisting of four IBRs is focused. The topology of this 4-IBR system is shown in Figure 32. This system can be seen as a combination of two paralleled systems studied in Section 2.3. Thus, the equations derived in the study in Section 2.3 can be reused for the multi-IBR system. Each paralleled VSG-GFLI system is referred to as a cluster. These two clusters are connected to a global common bus, whose voltage is $v_c\angle 0$, via transmission lines presented by $Z_{c,1}$ and $Z_{c,2}$. The global common bus is also connected to an infinite bus, representing the rest of the power system, via a grid impedance. Each cluster is formed by a VSG and a GFLI, which are connected to a local common bus, i.e., common bus 1 and common bus 2, via impedances. The voltages at the local common buses are $v_1\angle\delta_{v,1}$ for cluster 1 and $v_2\angle\delta_{v,2}$ for cluster 2.

The configurations of the GFLIs are identical to those presented in Section 2.3, while the VSG model is adopted from the study in Section 2.2 with a q-CL included.

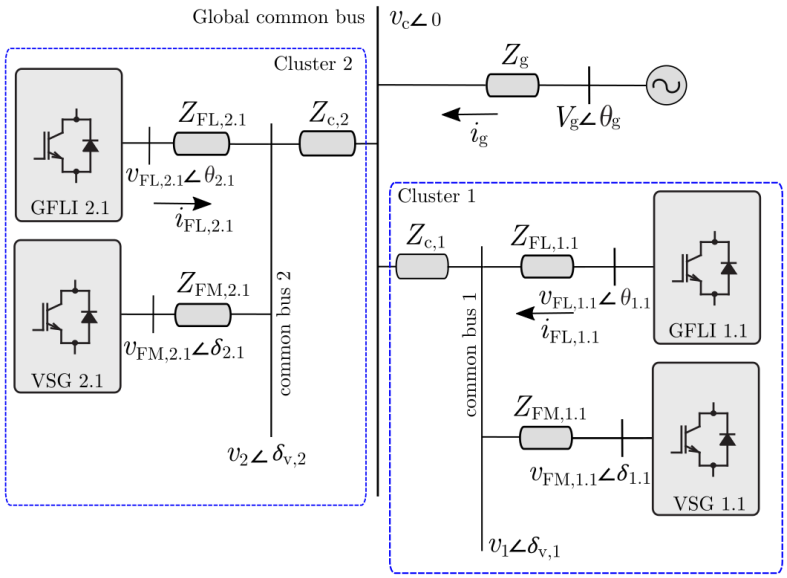


Figure 32. System diagram of the 4-IBR system.

### 2.5.2. Estimation of the distance between the SEP and the UEP

To measure the distance between the SEP and the UEP of a system, the first step is identifying these two equilibrium points (EPs). An EP is a state in a system where the net change or the rate of change is zero. In other words, it is a point in a dynamic system where the system remains unchanged over time. Since the operating point of the system is characterised by the power angles and voltage angles, as shown in (4) and the analysis in Section 2.3, an EP is where the rates of change of the angles are all zero. Thus, an EP is where the internal frequencies of the IBRs remain unchanged and equal the nominal frequency of the grid. This is where the active power of the VSGs equals their reference, and the q-voltage of the GFLIs converges to zero due to the tracking action of PLLs. Therefore, at an EP,

$$\begin{cases} P_{\mathrm{VSG},h.n} = P_{0,h.n} \\ v_{\mathrm{FLq},h.m} = 0, \end{cases} \tag{8}$$

where $P_{\mathrm{VSG},h.n}$ and $P_{0,h.n}$ are the electrical power and the reference power of VSG $h.n$ in cluster $h$. $v_{\mathrm{FLq},h.m}$ is the q-component of the voltage measured at the PoC of GFLI $h.m$ in cluster $h$. It is shown in [8] and Section 2.3.2 that (8) is equivalent to

$$\begin{cases} v_h = V_{\mathrm{c,VSG},h.n} \\ v_h = V_{\mathrm{c,GFLI},h.m} \end{cases} \tag{9}$$

where $v_h$ is the voltage at the local common bus $h$ in cluster $h$, $V_{\mathrm{c,VSG},h.n}$ and $V_{\mathrm{c,GFLI},h.m}$ are the critical values of $v_h$ and are derived in Appendix A1. $V_{\mathrm{c,VSG},h.n}$ and $V_{\mathrm{c,GFLI},h.m}$ are functions of the power angles and voltage angles, i.e., $\delta_{h.n}$ and $\theta_{h.m}$, and $v_h \angle \delta_{\mathrm{v},h}$. If $v_h = V_{\mathrm{c,VSG},h.n}$, the VSG $h.n$ is at one of its EPs. Likewise, when $v_h = V_{\mathrm{c,GFLI},h.m}$, the OP of the GFLI $h.m$ reaches one of its EPs. Therefore, eq. (9) is satisfied when cluster $h$ reaches an EP.

By applying the nodal analysis on cluster $h$, an expression for $v_h \angle \delta_{\mathrm{v},h}$ can be obtained as

$$\begin{cases} v_h = g(\delta_{h.n}, \theta_{h.m}) \\ \delta_{\mathrm{v},h} = l(\delta_{h.n}, \theta_{h.m}) \end{cases}. \tag{10}$$

The derivation of (10) is detailed in Appendix A2. Combining (9) and (10) gives an equation system consisting of four equations with four unknowns, i.e., $v_h$, $\delta_{\mathrm{v},h}$, $\delta_{h.n}$, and $\theta_{h.m}$, as

$$\begin{cases} v_h = V_{\mathrm{c,VSG},h.n} \\ v_h = V_{\mathrm{c,GFLI},h.m} \\ v_h = g(\delta_{h.n}, \theta_{h.m}) \\ \delta_{\mathrm{v},h} = l(\delta_{h.n}, \theta_{h.m}) \end{cases}. \tag{11}$$

With a given arbitrary value of the global common bus voltage, i.e., $v_{\mathrm{c}}$, an SEP and a UEP candidate of cluster $h$, if existing, can be determined by solving (11) for $v_h$, $\delta_{\mathrm{v},h}$, $\delta_{h.n}$, and $\theta_{h.m}$. ($v_{h,\mathrm{uep}}$, $\delta_{\mathrm{v},h,\mathrm{uep}}$,$\delta_{h.n,\mathrm{uep}}$, $\theta_{h.m,\mathrm{uep}}$) represents the root of (11) when the system is at a UEP candidate, while ($v_{h,\mathrm{sep}}$, $\delta_{\mathrm{v},h,\mathrm{sep}}$, $\delta_{h.n,\mathrm{sep}}$, $\theta_{h.m,\mathrm{sep}}$) denotes the root of (11) at an SEP candidate. System (11) can be solved by employing the MATLAB function `fsolve` or `vpasolve`.

In a properly designed system, at an SEP, the values of the common bus voltages, i.e., $v_{\mathrm{c}}$ and $v_h$, should be maintained above 0.85 pu. In contrast, these voltage values are supposed to be lower than 0.85 pu at the UEP of a properly designed system. Therefore, setting the searching range of the voltage values below/above 0.85 pu, when solving (11), allows obtaining the SEP/UEP.

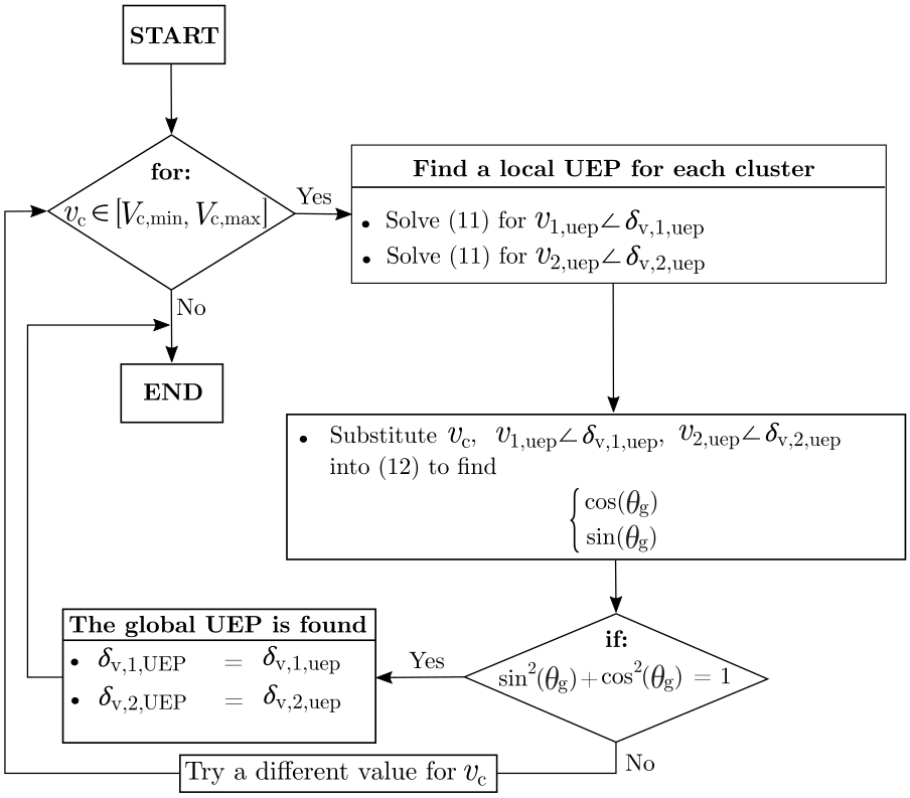


Figure 33. Flowchart the procedure for identifying the global UEP.

A flowchart representing the process to estimate the UEP of the system is shown in Figure 33. With a given $v_c$ value below 0.85 pu and $v_h$'s searching range below 0.85 pu, solving (11) for $v_h$ and $\delta_{v,h}$ gives a UEP candidate, i.e., ($v_{h,uep}$, $\delta_{v,h,uep}$), for cluster $h$. For each $v_c \in [V_{c,min}, V_{c,max}]$, where $0 < V_{c,min} < V_{c,max} < 0.85$ pu, one ($v_{1,uep}$, $\delta_{v,1,uep}$) pair and one ($v_{2,uep}$, $\delta_{v,2,uep}$) pair are determined for cluster 1 and cluster 2 respectively.

A set of ($v_{1,uep}$, $\delta_{v,1,uep}$, $v_{2,uep}$, $\delta_{v,2,uep}$) at a $v_c$ value forms a candidate for the actual UEP of the system. One more condition needs to be satisfied before concluding if the UEP candidate is the actual UEP of the whole system. Applying the nodal analysis on the global common bus and the local common buses, and rearranging result in

$$\begin{cases} \cos(\theta_g) = p(v_1, \delta_{v,1}, v_2, \delta_{v,2}) \\ \sin(\theta_g) = q(v_1, \delta_{v,1}, v_2, \delta_{v,2}) \end{cases}. \quad (12)$$

Eq. (12) shows how the grid voltage angle, i.e., $\theta_g$, with respect to the global common bus varies when the voltages at the local common buses change. More details of (12) are available in Appendix A3. If a UEP candidate is the actual global UEP of the system, when substituting ($v_{1,uep}$, $\delta_{v,1,uep}$, $v_{2,uep}$, $\delta_{v,2,uep}$) into (12) for $(v_1, \delta_{v,1}, v_2, \delta_{v,2})$, the resulting $\cos(\theta_g)$ and $\sin(\theta_g)$ must satisfy

$$\sin^2(\theta_g) + \cos^2(\theta_g) = 1. \quad (13)$$

If the aforementioned condition is not held, another $v_c \in [V_{c,min}, V_{c,max}]$ is tried, and the process is repeated. Otherwise, the UEP candidate is the actual UEP of the system and denoted as ($v_{1,UEP}$, $\delta_{v,1,UEP}$, $v_{2,UEP}$, $\delta_{v,2,UEP}$).

A similar process can be conducted with $0.85\ \text{pu} < V_{\text{c,min}} < V_{\text{c,max}}$ to identify the SEP. The actual SEP of the whole system is presented by ($v_{1,\text{SEP}}$, $\delta_{\text{v,1,SEP}}$, $v_{2,\text{SEP}}$, $\delta_{\text{v,2,SEP}}$). It is worth noting that the SEP of interest should belong to the normal voltage-controlled mode, while the UEP is expected to be in a current limited mode. Therefore, eq. (11) for estimating the SEP is different from the counterpart employed to identify the UEP. The component equations of (11) in this case can be found in [8]. Apart from that, the process is identical.

After estimating the SEP and the UEP of the system, the distance between these two EPs is estimated as below,

$$D_{\text{EP}} = \sqrt{\left(\frac{\delta_{\text{v,1,SEP}} - \delta_{\text{v,1,UEP}}}{\delta_{\text{v,1,SEP}}}\right)^2 + \left(\frac{\delta_{\text{v,2,SEP}} - \delta_{\text{v,2,UEP}}}{\delta_{\text{v,2,SEP}}}\right)^2}. \quad (14)$$

The distances between the SEP angles, i.e., $\delta_{\text{v,1,SEP}}$ and $\delta_{\text{v,2,SEP}}$, and the UEP angles, i.e., $\delta_{\text{v,1,UEP}}$ and $\delta_{\text{v,2,UEP}}$, are normalised by dividing the differences between these two points by the SEP angles in calculating the $D_{\text{EP}}$. The higher the value of $D_{\text{EP}}$ is, the further the SEP and the UEP of the system is apart from each other, hence more stable the system is.

### 2.5.3. Estimation of the distance between the SEP and the voltage control instability

As presented in Section 2.2, when a q-CL is employed, there is a possibility that there is no UEP existing in the synchronising loop of the VSGs. Thus, the global UEP might not always exist. The absence of the UEP in the synchronising loop is caused by the disappearance of an SEP in the voltage control loop. Hence, the VSG might become unstable due to the instability of the voltage loop before its OP reaches the UEP. In these cases, instead of focusing on finding the UEP, estimating the closest location, where at least one VSG fails due to the voltage loop instability, to the SEP is more practical.

When there is no UEP existing in the system, the condition in (13) is not satisfied by any value of $v_{\text{c}}$ below 0.85 pu. To obtain an index that is similar to the distance between the SEP and the UEP, a replacement for the UEP in the calculation needs to be derived. Studying the behaviours of the end point introduced in Section 2.2 is the direction to proceed in.

#### 2.5.3.1 The end point of the power-angle curve of a q-CL-VSG, considering voltage variations

In this subsection, a small SMIB model as shown in Figure 34 is investigated.

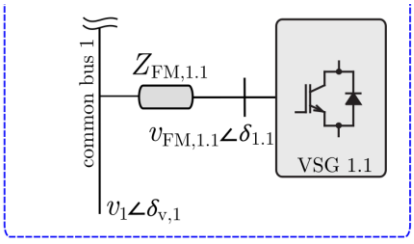


Figure 34. A SMIB model of the VSG in Cluster 1

As shown in Section 2.2, the end point of a q-CL-VSG is its power angle limit, where the power angle cannot stably further increase. In severe transients, excessive angle growths are restrained and

capped at the end point or the end point angle, i.e., $\delta_c$. If the end point is above the reference power $P_0$, (Case II in Figure 6), no UEP in the power-angle loop exists. When the OP of any VSG reaches its instantaneous end point, it stays there until the voltage loop becomes unstable. This case usually occurs when $P_0$ is low. However, the end point in this analysis is varying due to the variations of the voltage at the most immediate bus since $\delta_c$ is inversely proportional to this voltage magnitude, $v_1$. Therefore, the end point of a VSG varies during transients. It evolves to the right and reduces in terms of power as $v_1$ decreases, as shown in Figure 35. The movement of the end point to the right (higher $\delta_c$) postpones the instability of the voltage loop. At high values of $v_1$, the OP easily reaches the end point due to low $\delta_c$ values. If the transients are severe and $P_0$ is low, the OP follows the evolution of the end point until $v_1$ is low enough and the UEP of the power-angle control is restored. At this instant, the end point, followed by the OP, reaches and exceeds the UEP of the power angle control of the VSG. Hence, the power-angle control loop enters a positive feedback mode and becomes unstable.

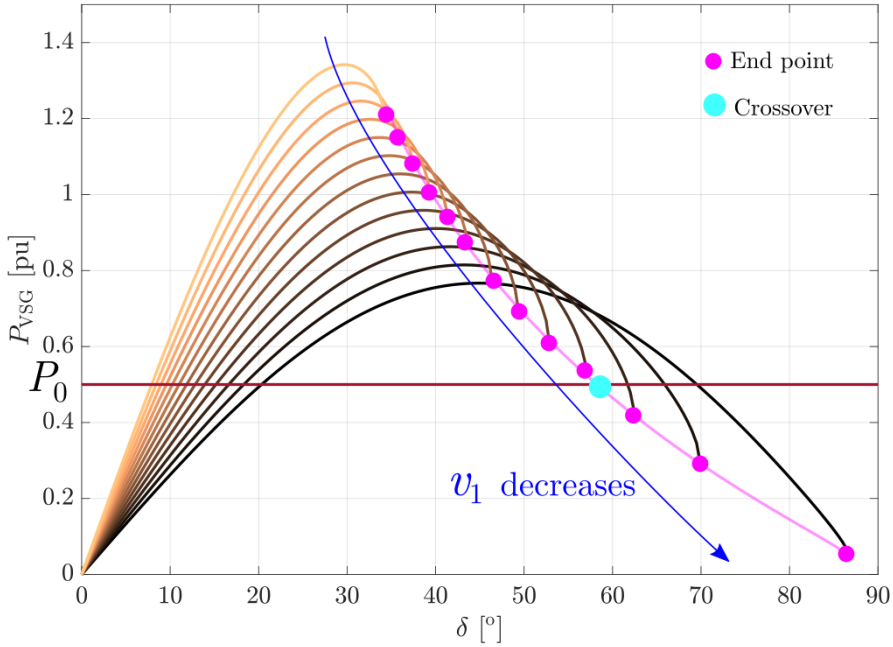


Figure 35. Power-angle curves of the current-limited mode of a q-CL-VSG when $v_1$ decreases.

Therefore, if there is no UEP existing in a multi-IBR system, the point where the end point of any VSG drops below its $P_0$ is the replacement for the global UEP. This point is referred to as the crossover point of the end point and $P_0$ or the crossover point for short.

#### 2.5.3.2 Identifying the crossover point of the end point and $P_0$

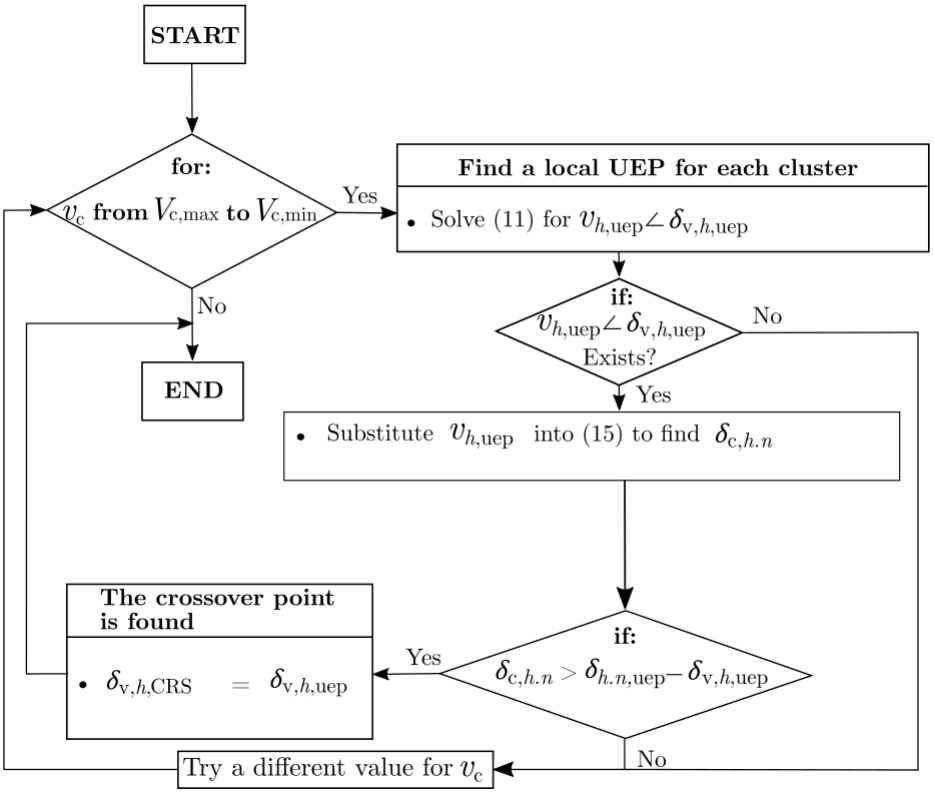


Figure 36. Flowchart the procedure for identifying the crossover point when no UEP exists.

After completing the process in Figure 33, if there is no global UEP existing (or eq. (13) is not satisfied), the process in Figure 36 is run to find the crossover point for each cluster. For each value of $v_c$, the end point's angle of VSG $h.n$ in cluster $h$, denoted as $\delta_{c,h.n}$, is

$$\delta_{c,h.n} = \sin^{-1}\left(\frac{I_{max,h.n} Z_{FM,h.n}}{v_{h,uep}}\right). \quad (15)$$

It is necessary to note that $v_{h,uep}$ and $\delta_{c,h.n}$ might not always exist for every $v_c$ value. When $v_c$ is low enough, the UEP is restored, and $\delta_{c,h.n}$ can be identified. $\delta_{c,h.n}$ is then checked against $\delta_{h.n,uep}$. If $\delta_{c,h.n} > (\delta_{h.n,uep} - \delta_{v,h,uep})$, indicating that the end point of VSG $h.n$ drops below its $P_0$, the crossover point of cluster $h$ is found. The value ($v_{h,uep}$, $\delta_{v,h,uep}$) at this point is assigned to the crossover point of cluster $h$, i.e., ($v_{h,CRS}$, $\delta_{v,h,CRS}$).

The distance between the EPs is replaced by the distance between the SEP and the crossover point as derived below,

$$D_{EP} = \sqrt{\left(\frac{\delta_{v,1,SEP} - \delta_{v,1,CRS}}{\delta_{v,1,SEP}}\right)^2 + \left(\frac{\delta_{v,2,SEP} - \delta_{v,2,CRS}}{\delta_{v,2,SEP}}\right)^2}. \quad (16)$$

### 2.5.4. Validations

In this section, the $D_{EP}$ discussed above is validated in measuring the transient stability of the 4-IBR system presented in Figure 32 above. Several test cases, whose parameters are listed in Tables 3-5 below, are conducted. In each case, power references and grid impedances are varied and the $D_{EP}$

of the case is calculated and compared with that of other cases. A higher $D_{\mathrm{EP}}$ indicates a more stable system, which can withstand longer faults and remain stable.

The base voltage and base power of the test cases are 110 kV and 55 MVA respectively. Faults are applied at t = 8 s. The fault location is between the global common bus and the infinite bus.

**Table 3. Multi-IBR study: parameters of the clusters.**

| | |
|---|---|
| $I_{\mathrm{max},1.1}$ | 1.35 (pu) |
| $I_{\mathrm{max},2.1}$ | 1.40 (pu) |
| $Z_{FM,1.1}$ | 0.11 (pu) |
| $Z_{FL,1.1}$ | 0.06 (pu) |
| $Z_{FM,2.1}$ | 0.13 (pu) |
| $Z_{FL,2.1}$ | 0.08 (pu) |

### Variations of the active power reference of VSG 1.1

**Table 4. Multi-IBR study: simulation parameters of Cases a, b, and c.**

| Case | $P_{0,1.1}$ (pu) | $P_{0,2.1}$ (pu) | $Z_{c,1}$ (pu) | $Z_{c,2}$ (pu) | $D_{\mathrm{EP}}$ | Fault duration (ms) |
|---|---|---|---|---|---|---|
| a | 0.85 | 0.93 | 0.17 | 0.17 | 1.31 | 268 |
| b | 0.92 | 0.93 | 0.17 | 0.17 | 1.18 | 268 |
| c | 0.67 | 0.93 | 0.17 | 0.17 | 1.22 | 268 |

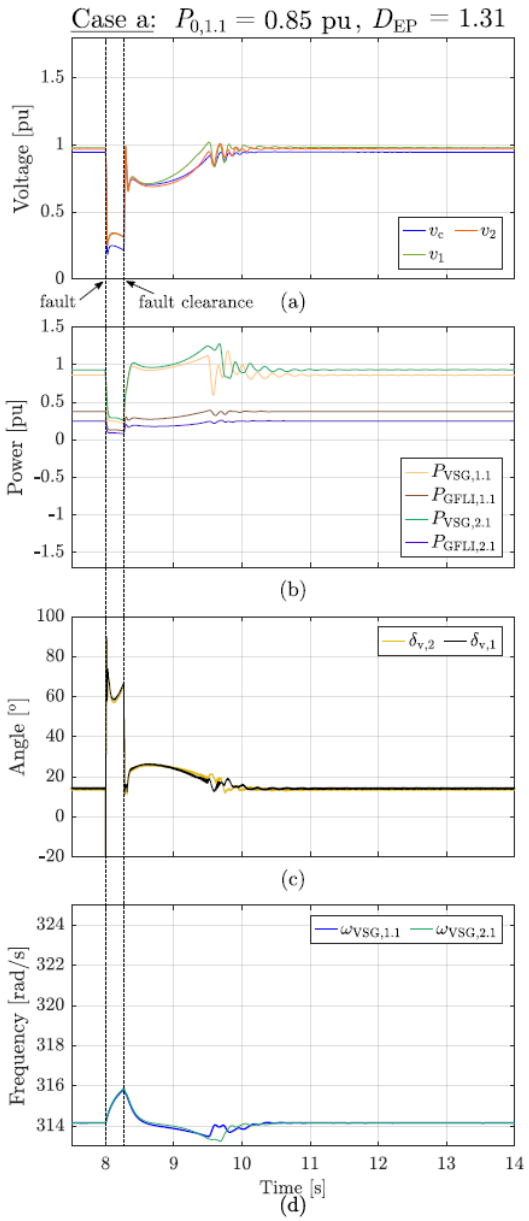


Figure 37. Multi-IBR study: Simulation results of Case a. (a) voltage measurements, (b) power measurements, (c) angle measurements, and (d) frequency measurements.

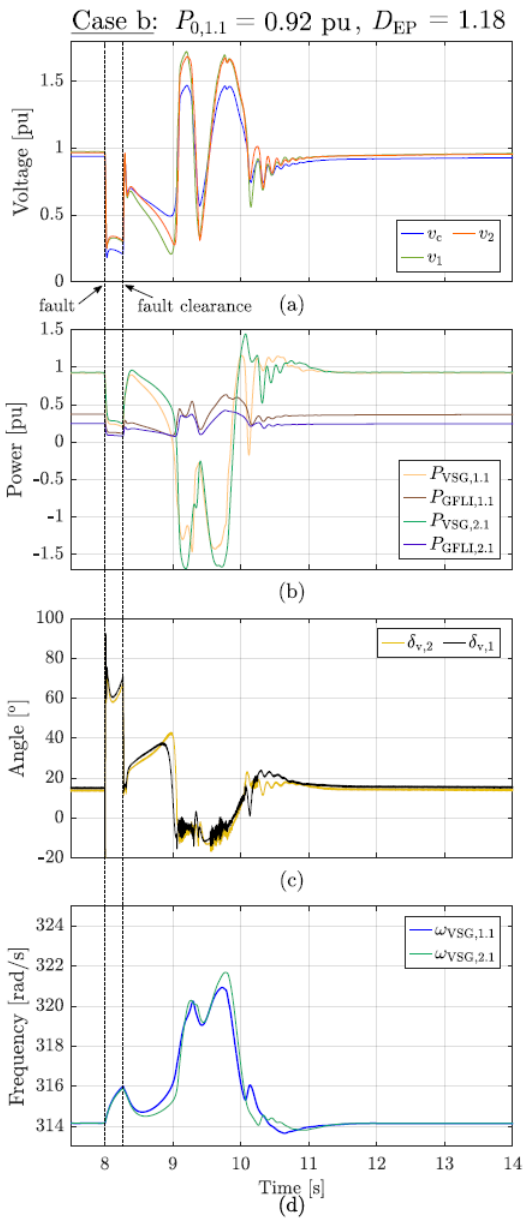


Figure 38. Multi-IBR study: Simulation results of Case b. (a) voltage measurements, (b) power measurements, (c) angle measurements, and (d) frequency measurements.

From Table 4, it is shown that an increase in the active power reference of VSG 1.1, i.e., $P_{0,1.1}$, results in a reduction of the $D_{\mathrm{EP}}$ from 1.31 in Case a to 1.18 in Case b. This indicates a deterioration in the transient stability of the 4-IBR system when the power setpoint is increased. This conclusion is verified by the time-domain simulations shown in Figures 37 and 38. With the same fault duration of 268 ms, which is also the critical clearing duration of Case a, the system in Case a with higher $D_{\mathrm{EP}}$ remains stable and converges to a new steady-state without significant transients in the responses, while the system in Case B becomes unstable in the first post-fault swing. After the fault clearance, the power, voltage, and frequency of the system in Case B deviate to extreme values, which can lead to an isolation of the IBRs from the network by the protection system. As there is no protection system implemented in the simulation, the system in Case b can return a stable operation from the second swing onwards.

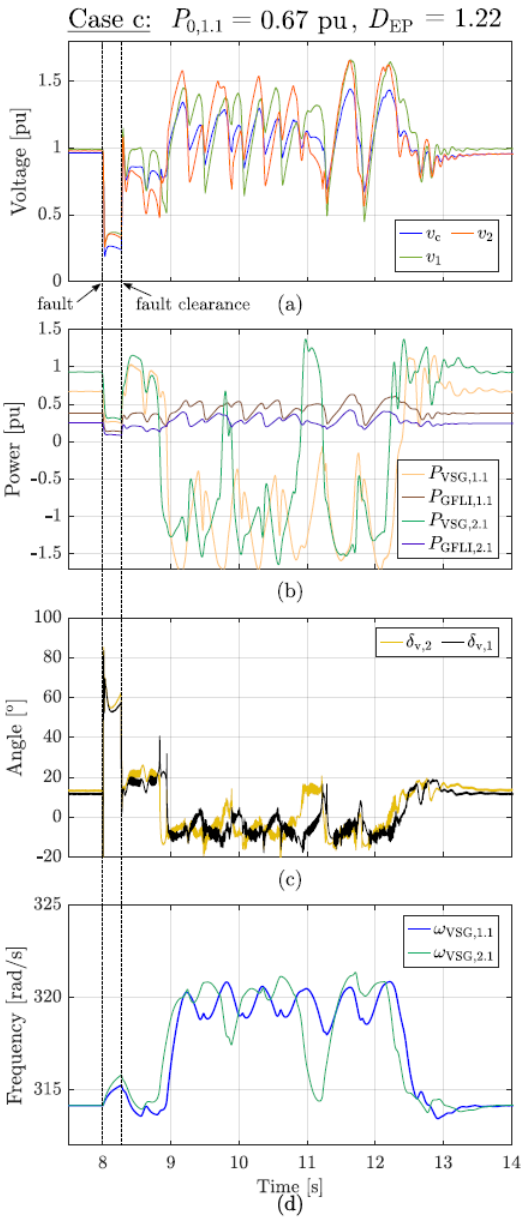


**Figure 39. Multi-IBR study: Simulation results of Case c. (a) voltage measurements, (b) power measurements, (c) angle measurements, and (d) frequency measurements.**

From the comparison between Case a and Case b, it is expected that a lower $P_{0,1.1}$ results in a higher stability margin, thus, a higher $D_{EP}$. Nevertheless, in Case c when $P_{0,1.1}$ is reduced to 0.67 pu, $D_{EP}$ drops to 1.22. Hence, the time-domain responses become unstable after the fault clearance in Case c. The instability in this case is supposed to be caused by the instability of the voltage control loop in VSG 1.1, as analysed in Section 2.2. Therefore, the $D_{EP}$ values of the three cases discussed above align with the time-domain simulations and can represent the stability margin of the 4-IBR system.

### Variations of grid impedances

Table 5. Multi-IBR study: simulation parameters of Cases d, e, f, and g.

| Case | $P_{0,1.1}$ (pu) | $P_{0,2.1}$ (pu) | $Z_{c,1}$ (pu) | $Z_{c,2}$ (pu) | $D_{EP}$ | Fault duration (ms) |
|---|---|---|---|---|---|---|
| d | 0.85 | 0.93 | 0.17 | 0.17 | 1.31 | 260 |
| e | 0.85 | 0.93 | 0.27 | 0.17 | 1.10 | 260 |
| f | 0.85 | 0.93 | 0.27 | 0.17 | 1.10 | 257 |
| g | 0.85 | 0.93 | 0.17 | 0.27 | 0.85 | 257 |

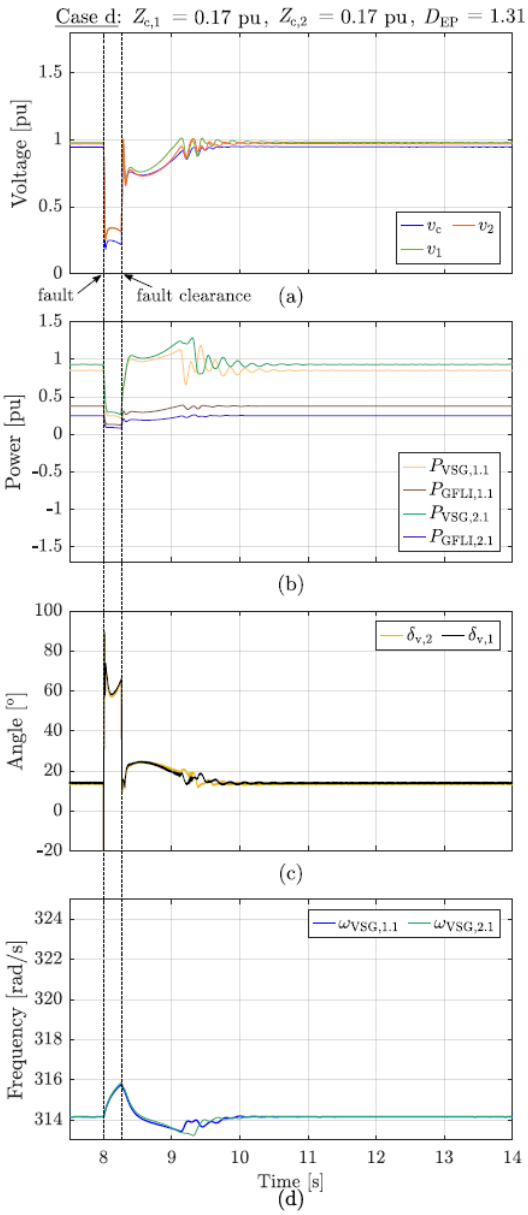


Figure 40. Multi-IBR study: Simulation results of Case d. (a) voltage measurements, (b) power measurements, (c) angle measurements, and (d) frequency measurements.

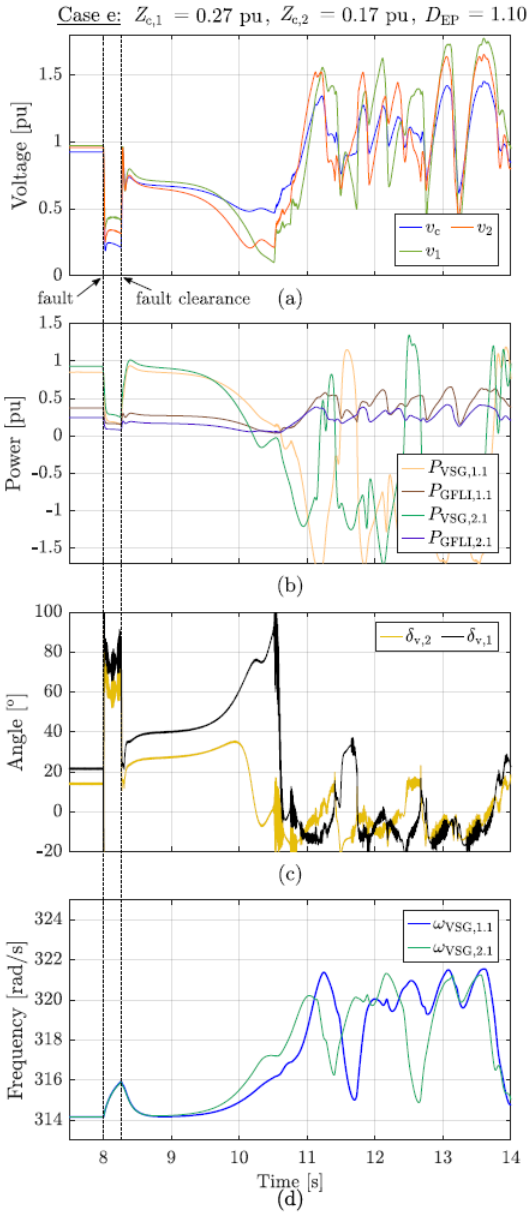


Figure 41. Multi-IBR study: Simulation results of Case e. (a) voltage measurements, (b) power measurements, (c) angle measurements, and (d) frequency measurements.

Parameters of Cases d, e, f, and g are summarised in Table 5. In Case d, the impedance of the line connecting cluster 1 to the global common bus, i.e., $Z_{c,1}$, is kept at 0.17 pu, while it is increased to 0.27 pu in Case e to emulate a line tripping. Due to the reduction in terms of power transfer capability caused by the line impedance rise, $D_{EP}$ drops from 1.31 in Case d to 1.10 in Case e. This

deterioration of the stability is validated by the time-domain simulations presented in Figures 40 and 41. The system in Case d with the higher $D_{\mathrm{EP}}$ remains stable, while that in Case e becomes unstable after the fault clearance.

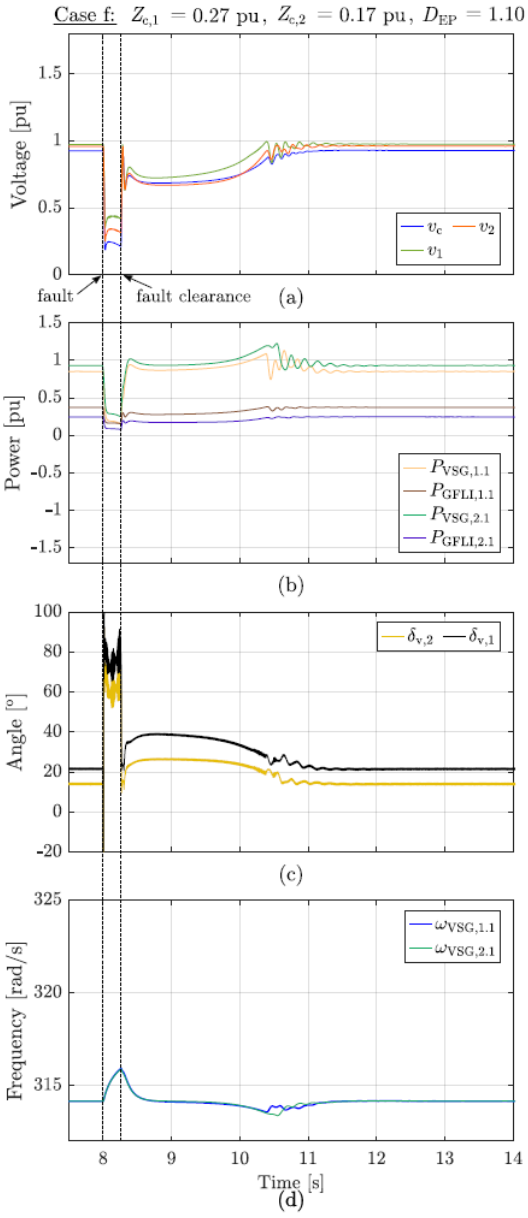


Figure 42. Multi-IBR study: Simulation results of Case f. (a) voltage measurements, (b) power measurements, (c) angle measurements, and (d) frequency measurements.

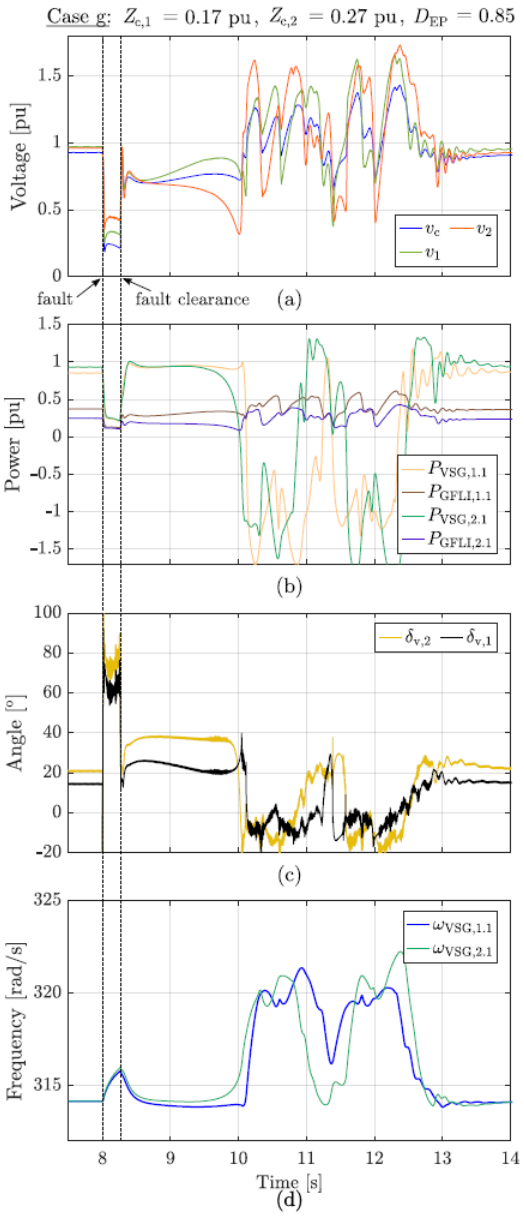


Figure 43. Multi-IBR study: Simulation results of Case g. (a) voltage measurements, (b) power measurements, (c) angle measurements, and (d) frequency measurements.

Moreover, the $D_{\mathrm{EP}}$ can also show how stable a cluster is, compared to the other cluster in the 4-IBR system. In Case e above, a line tripping leading to a rise of $Z_{\mathrm{c},1}$ to 0.27 pu, results in a $D_{\mathrm{EP}}$ of 1.10 for the 4-IBR system. Nevertheless, it is shown that the stability of the system is even degraded more significantly if the line tripping occurs between cluster 2 and the global common bus instead. In Case g, the line tripping location is moved to the line between the global common bus and cluster 2. This is indicated by a rise to 0.27 pu in $Z_{\mathrm{c},2}$. This change causes a drop to 0.85 in the $D_{\mathrm{EP}}$. Hence, the

system in Case g is expected not to be as stable as that when the line tripping occurs in cluster 1. In Case f, the fault duration is reduced to 257 ms, which was 260 ms in Case e, to keep the system stable when $Z_{c,1}$ =0.27 pu. Since the $D_{EP}$ in Case g is lower than that in Case f, the responses of the system in Case g are expected to experience more extreme transients. This is verified by the time-domain results presented in Figures 42 and 43.

### Variations of the active power reference of VSG 2.1

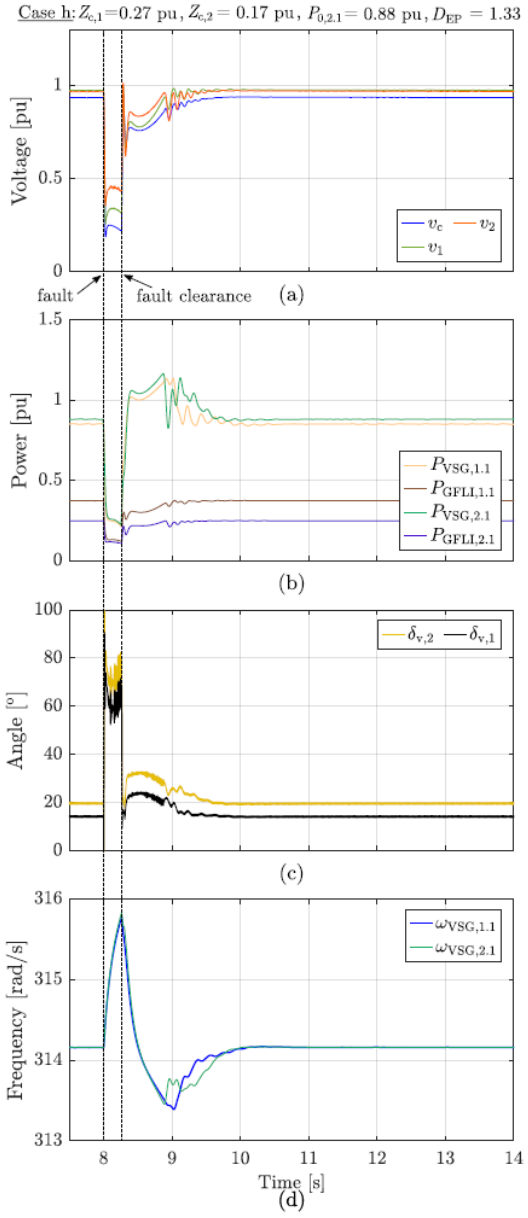


Figure 44. Multi-IBR study: Simulation results of Case h. (a) voltage measurements, (b) power measurements, (c) angle measurements, and (d) frequency measurements.

Table 6. Multi-IBR study: simulation parameters of Cases d and h.

| Case | $P_{0,1.1}$ (pu) | $P_{0,2.1}$ (pu) | $Z_{c,1}$ (pu) | $Z_{c,2}$ (pu) | $D_{EP}$ | Fault duration (ms) |
|---|---|---|---|---|---|---|
| d | 0.85 | 0.93 | 0.17 | 0.17 | 1.31 | 260 |
| h | 0.85 | 0.88 | 0.17 | 0.27 | 1.33 | 260 |

A growth in the $Z_{c,2}$ limits the power transfer capability of the transmission line. Therefore, reducing power transferred over the line between the global common bus and cluster 2 is beneficial for the system stability. In Case h, the active power reference of VSG 2.1 is reduced to 0.88 pu. This reduction brings the $D_{EP}$ to 1.33, which is even higher than that of the original Case d, where both $Z_{c,1}$ and $Z_{c,2}$ are 0.17 pu. Hence the system in Case h is expected to be at least as stable as that in Case d. The aforementioned improvement is validated by the time-domain simulation shown in Figure 44. In Case h, the same fault and fault duration as these in Case d are applied. The system in Case h with the reduction in $P_{VSG,2.1}$ can stably recover as that in Case d does, although $Z_{c,2}$ is set to 0.27 pu in Case h.

### 2.5.5. Applications of the study

As shown above, the $D_{EP}$ developed for the 4-IBR network can be utilised as a transient stability margin indicator. It can quickly show how stable a system is when there are changes in the system. Moreover, it allows comparing the stability margin of different systems. This is beneficial for system design and operation. For example, for a given network, one can investigate the importance of certain lines in the network. If one of them is disconnected, how severely that will impact the stability of the whole system. Based on that understanding, recommendations for remedial asset installations, such as new transmission lines, Synchronous condensers, can be given. In addition, operational limits for IBRs in different clusters or regions to maintain a certain level of stability can be determined by the study above. The significance of this study is that it takes the non-linear current limitation of VSGs into consideration when investigating the transient stability to provide a more accurate stability measurement.

An automating script can be built following the processes presented in Section 2.5.3. This script prompts the system parameters, e.g., line impedances, power dispatch levels, and current limits, to estimate the stability margin of the system via the $D_{EP}$. The extension of this study to a larger system and the development of a plug-and-play automating script (with a user interface) are within the scope of future works of this study.

## 2.6. GFMI's Functionality Tests

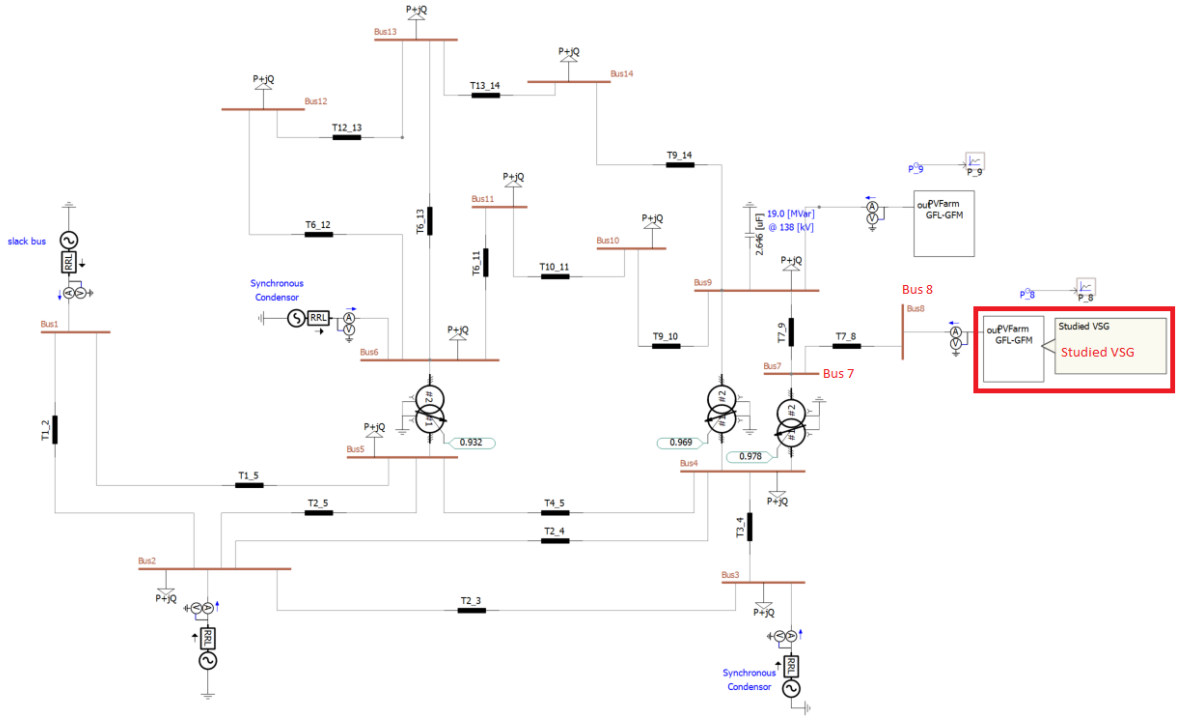


Figure 45. Tested system of the functionality tests.

In this section, IBRs equipped with the controls introduced in Sections 2.2 and 2.4 will be examined in fault conditions. The performance of the IBRs will be evaluated based on the requirements and standards, i.e., IEEE P2800 and NERC PCR-024-2, summarised in the white paper mentioned in Section 2.1. The IBRs will be tested against the no-trip zone and the response speed requirements specified in that white paper. The aim of this task is to evaluate the improvements brought by the aforementioned controls. Besides, shortcomings of these auxiliary controls might be revealed in these tests. Thus, recommendations for improvements can be given.

### 2.6.1. System Configurations of the Functionality Tests

An IEEE 14-bus system as shown in Figure 45 is employed in this task. A GFMI with VSG control is connected to Bus 8 of this system to support a nearby GFLI-based solar farm. The GFMI's internal structure is presented in the white paper presented in Section 2.1 and in [13]. The simulations are conducted in PSCAD/EMTDC. The base voltage and base power of the simulations are 138 kV and 100 MVA respectively. Five test cases, whose parameters are listed in Table 7, are conducted in this section.

For each tested case, RMS and q-component of the PoC voltage (Vrms_PoC and Vq), active and reactive powers (P and Q), d- and q-components of the line current (Id and Iq), and the VSG frequency traces are presented in Figures 46-50. It should be noted that, in all figures:

- the trace colour serves as a means of distinguishing between the outcomes of various CL methods,
- solid lines and the left y-axis correspond to RMS voltage, Id, P, and frequency traces,

- dashed lines and the right y-axis correspond to Vq, Iq, and Q traces.

**Table 7. Simulation parameters of the functionality tests**

| Test | $P_0$ (MW) | $V_{ref}$ (pu) | $T_{fault}$ (ms) | $L_{fault}$ (pu) | $R_{fault}$ (pu) | Fault Location | $I_{max}$ (pu) | Current Limitation Mode | Angle Freeze | Results |
|---|---|---|---|---|---|---|---|---|---|---|
| **Case 1** | 50 | 1.03 | 310 | 0.016 | 0.53e-4 | Bus 8 | 1.2 | q-CL, mod-q-CL | Off | Figure 46 |
| **Case 2** | 50 | 1.03 | 200 | 0.016 | 0.53e-4 | Bus 8 | 1.2 | mod-q-CL, d-CL | Off | Figure 47 |
| **Case 3** | 50 | 1.03 | 450 | 0.041 | 1.57e-4 | Bus 7 | 1.2 | mod-q-CL, d-CL | Off | Figure 48 |
| **Case 4** | 50 | 1.03 | 640 | 0.016 | 0.53e-4 | Bus 8 | 1.2 | mod-q-CL, d-CL | Off | Figure 49 |
| **Case 5** | 50 | 1.03 | 640 | 0.016 | 0.53e-4 | Bus 8 | 1.2 | mod-q-CL, d-CL | On | Figure 50 |

### 2.6.2. Functionalities to be Investigated

#### Modified q-prioritised CL

In this section, Case 1 is investigated. In this test, one symmetrical fault is applied at Bus 8 of the system for 310 ms. Two tests are conducted: with the conventional q-CL and with the modified q-CL (mod-q-CL) presented in Section 2.4. The applied fault results in a residual voltage of 0.2 pu at the PoC of the VSG during the fault. It is shown in Figure 46 that both q-CL and mod-q-CL respond almost immediately to the fault occurrence by raising their reactive power injections. In addition, the reactive power injections settle within 0.68 ms, which is less than 4 cycles of a 50-Hz system. Thus, these two cases comply with the IEEE Std. P2800 in terms of step response time and settling time. However, the q-CL becomes unstable after the fault clearance. The instability of the q-CL is caused by the failure of the voltage control loop as discussed in Section 2.2. On the other hand, the mod-q-CL can quickly allow the voltage to recover. Despite a few post-fault swings, the VSG and the system are able to return to a stable operation after 1.5 s since the fault clearance. Therefore, in this case, the improvement brought by the mod-q-CL can be validated. Moreover, the mod-q-CL satisfies the voltage ride-through capability (VRTC) requirement of NERC PCR-024-2 [14], which only requires the IBR to ride through a 150-ms fault with the residual voltage of 0.2 pu.

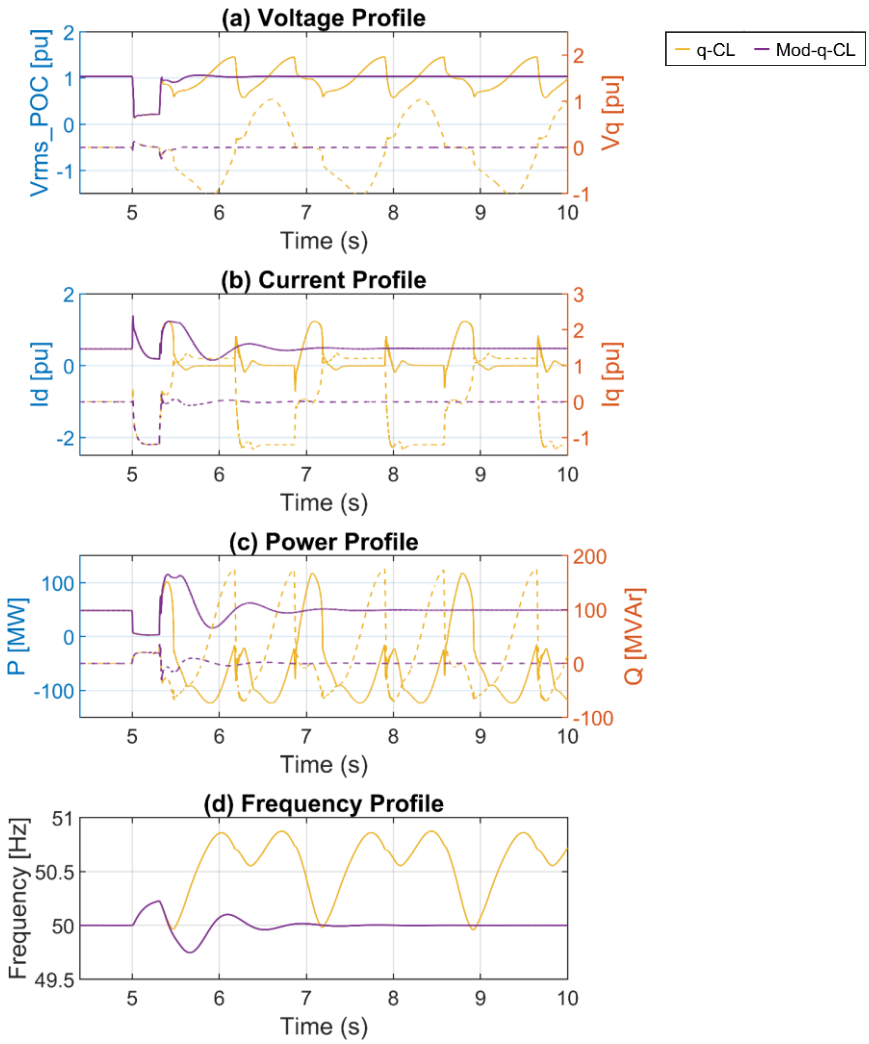


Figure 46. Functionality test: Simulation results of Case 1.

### d- and q- prioritised current limiter (CL) comparison

In this section, the performances of the d-CL and the mod-q-CL are compared. Cases 2, 3, and 4 are conducted to investigate the responses of VSGs equipped with d-CL and mod-q-CL. The results are summarised in Figures 47, 48, and 49.

In Case 2, a symmetrical fault is applied at Bus 8 to create a deep voltage sag at the PoC of the VSG. The fault lasts 200 ms to ensure that the VSG satisfies the VRTC requirement specified in the standard NERC PCR-024-2. Both d-CL and mod-q-CL can stably ride through and recover from the fault despite the low residual voltages at the PoC. However, as discussed in Section 2.2, the mod-q-CL (or q-CL in general) provides more voltage/reactive power support compared to the d-CL, as presented in Figures 47(a), and 47(c). The voltage and reactive power levels in the case equipped with mod-q-CL are higher than those in the case where d-CL is employed. These supports are beneficial for the network and nearby assets. The frequency deviation of the case with mod-q-CL is lower than that in the case with d-CL.

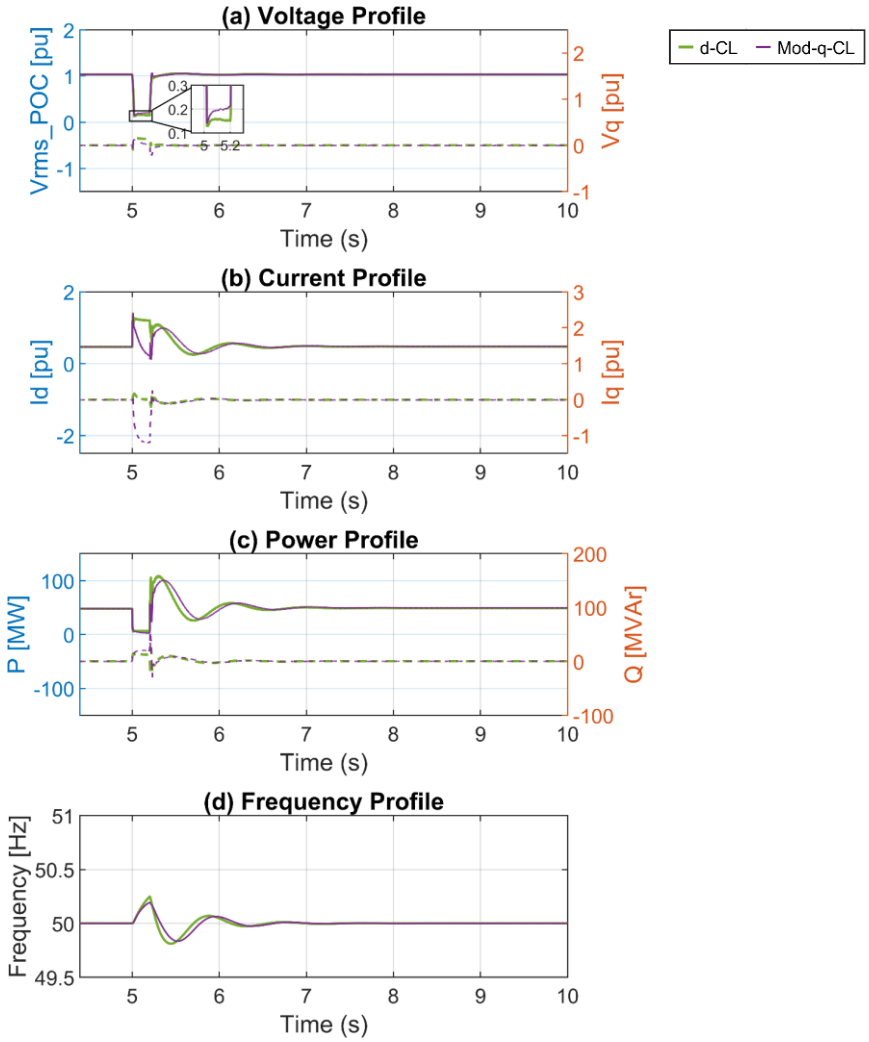


Figure 47. Functionality test: Simulation results of Case 2.

In Case 3, the fault is moved to Bus 7 to emulate a shallower fault for the VSG. The fault duration is set to 450 ms to make sure the VSG meets the VRTC required by the standard NERC PCR-024-2. Similarly to Case 2, both d-CL and mod-q-CL successfully ride through the fault and remain stable. Again, the mod-q-CL helps to inject more reactive power, thus maintain a higher voltage level at the PoC. However, as Id is strictly limited by mod-q-CL, active current used for synchronising the VSG with the grid is pushed to low values. Hence, the active power error fed to the synchronising loop of the VSG is higher in the case with mod-q-CL. This results in a greater frequency deviation as shown in Figure 48(d). Thus, the post-fault swing in the case with mod-q-CL is more severe compared to that in the case with d-CL.

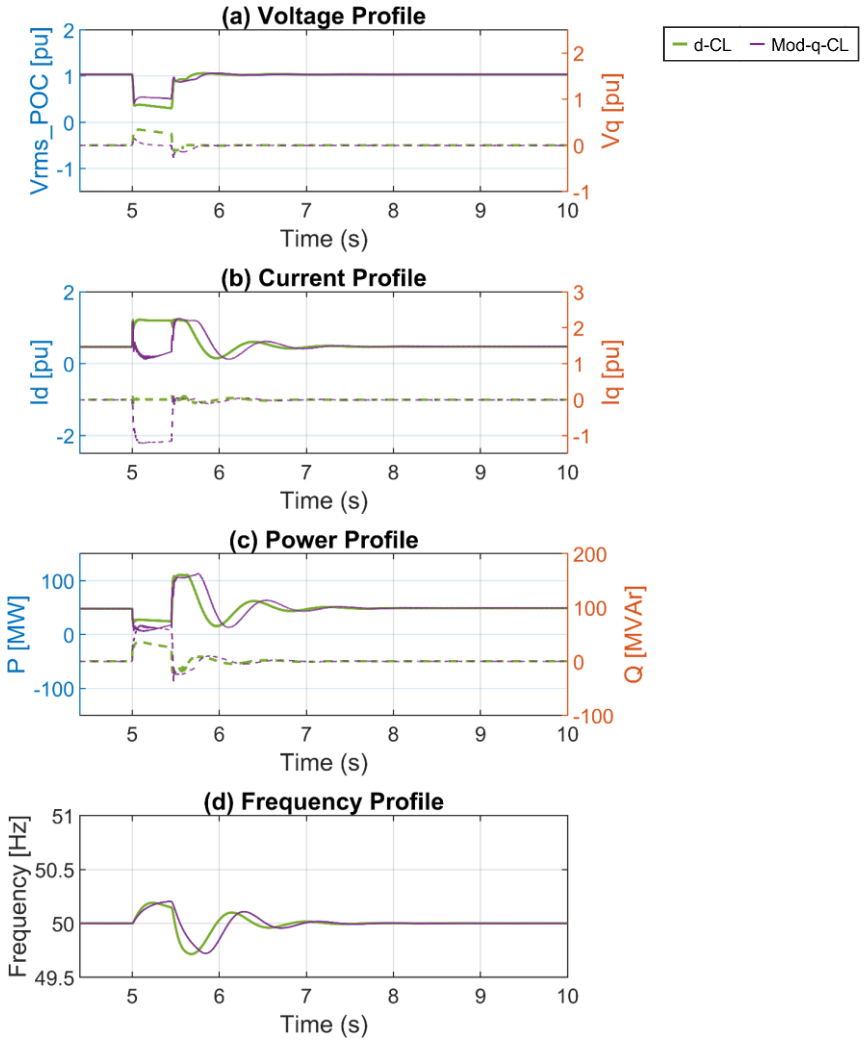


Figure 48. Functionality test: Simulation results of Case 3.

To explore and compare the stability limits of the d-CL and the mod-q-CL, Case 4, where the fault duration is set to 640 ms and the fault is applied right at the PoC of the VSG, i.e., Bus 8, is conducted. In this case, the VSG equipped with d-CL fails to return to an acceptable operation after experiencing an extremely severe power transient as shown in Figure 49. On the other hand, the mod-q-CL allows the VSG to recover to a stable operation with the voltage and power converging to the pre-fault conditions subsequently to post-fault swings. Therefore, the mod-q-CL offers higher stability margin than the d-CL does in this test.

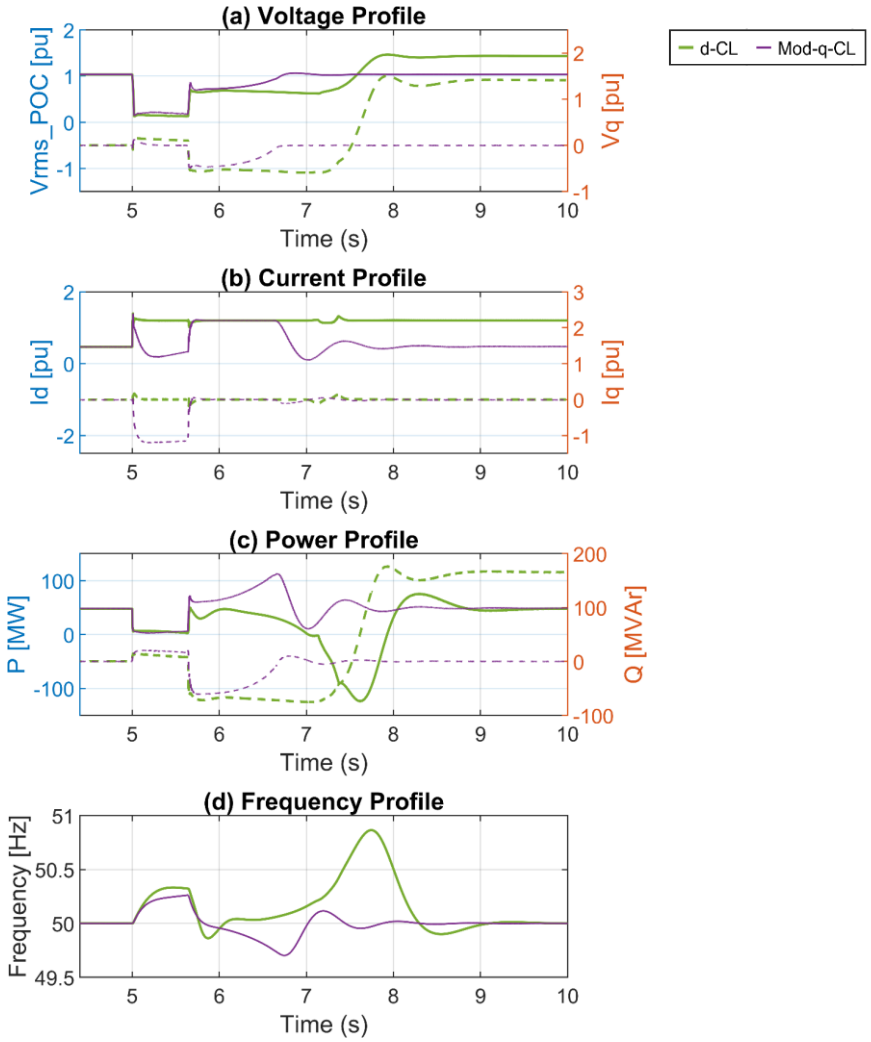


Figure 49. Functionality test: Simulation results of Case 4.

### Freezing Angle

In this section, the enhancement from the angle freezing scheme in stabilising the VSG during and subsequently to faults is validated. The tests in Case 4 above are repeated with the angle freezing scheme enabled in Case 5. The results of this test case are presented in Figure 50. With the angle freezing scheme active, the VSG equipped with d-CL can remain stable and return to the pre-fault operation, while its response without the angle freezing scheme in Case 4 is unacceptable. Moreover, the post-fault transient of the case with mod-q-CL is also considerably improved with the angle-freezing engagement.

However, the activation of the angle freezing scheme blocks the power error fed to the synchronising loop of the VSG, thus disabling this loop. Therefore, this scheme should only be employed in severe fault conditions to avoid interfering with the synchronising loop and the primary control of the VSG unnecessarily.

## 2.6.3. Summary

The mod-q-CL, which is a variant of the conventional q-CL as presented in Section 2.4, offers a higher transient stability margin compared to the q-CL, while retaining the high reactive power injection

feature of the q-CL during faults. The high reactive power support from the mod-q-CL (or q-CL) results in a higher in-fault voltage level at the PoC of the VSG compared to that of a VSG employing a d-CL. Hence, more voltage support from VSGs equipped with the mod-q-CL is expected. In contrast, mod-q-CL (or q-CL) pushes the limits of the d-current and active current to low values, thus leading to greater active power errors inputted to the synchronising loop of a VSG. In shallow faults, this might cause more extensive frequency deviations compared to the cases where d-CLs are employed.

Finally, in severe faults, the angle freezing scheme helps improve the transient stability of VSGs and their post-fault responses.

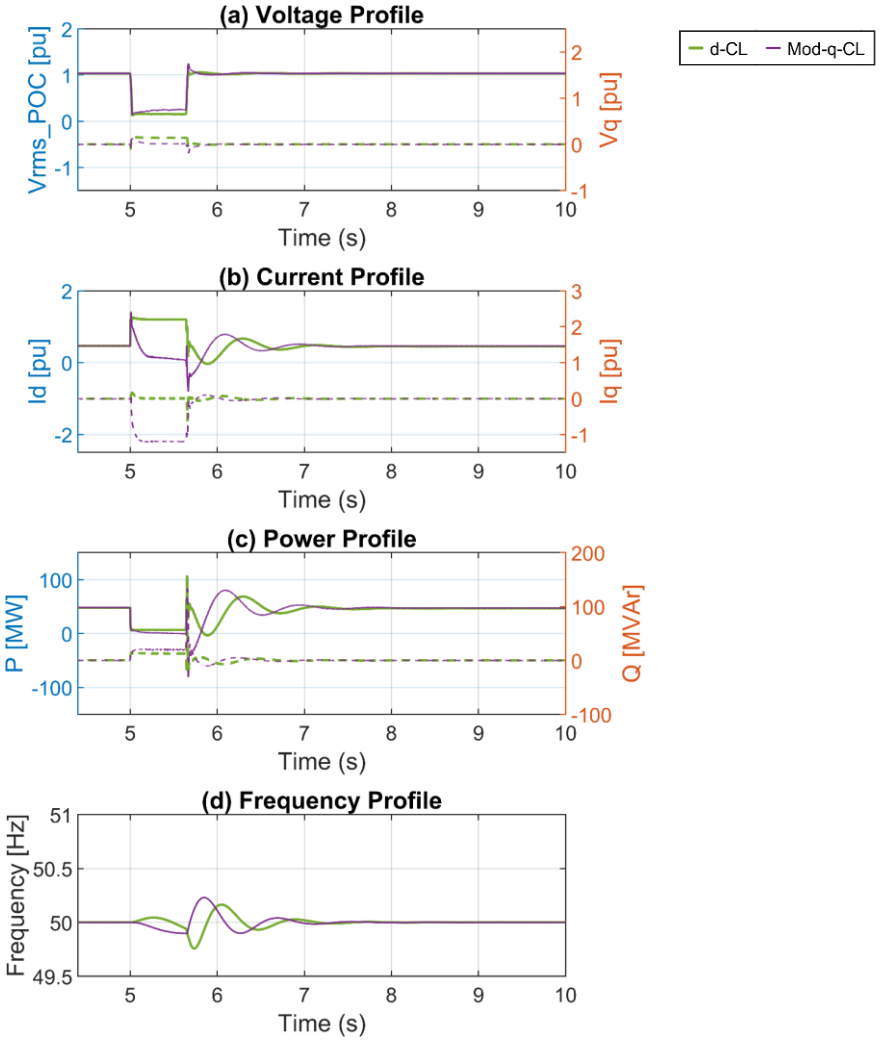


Figure 50. Functionality test: Simulation results of Case 5.

# 3. Conclusions

This report presents a comprehensive study that focuses on GFMIs in power systems, specifically their design, transient stability, and control enhancements. The primary objective of this research is to enhance the performance and reliability of IBRs in modern power systems. The project

encompasses a series of interconnected tasks, progressing from the specification of inverter design to the analysis of complex multi-IBR systems.

The research begins by thoroughly reviewing global grid codes and performance standards to derive design specifications for inverters that improve their ability to remain connected to the grid during large-signal disturbances. This forms the foundation for investigating the transient stability of GFMIs equipped with current limiters. These limiters are essential for protecting GFMIs from overcurrents but negatively impact their stability margin. The study highlights the significance of q-prioritised current limiters, commonly used in the industry.

Building on these insights, the research delves into the transient stability of paralleled systems, including both grid-forming and grid-following inverters. This analysis leads to the development of an adaptive power reference control (APRC) designed to enhance transient stability in various scenarios. Experimental evaluations conducted at Monash University demonstrate the effectiveness of the APRC in improving the damping and stability of paralleled systems.

Subsequently, the research extends its focus to multi-IBR systems, aiming to develop indices or indicators for quickly measuring transient stability margins. These indicators consider the distance between stable and unstable equilibrium points in the operating domain of the system. This analysis aims to provide an analysing tool for evaluating the performance and stability of complex power systems with multiple IBRs. The tool's output can offer indicators for the transient stability margin of a network. Preliminary studies have been conducted in developing the tool in stage 2, with plans to continue its development and enhance its computing process in stage 3.

The findings of this project can assist OEMs and IBR developers in quickly determining the stability limits of a grid-forming inverter when connecting it to a specific point of connection. This allows for proper design and understanding of the inverter's capabilities. Additionally, the proposed and investigated enhancing controllers in this stage can serve as recommendations for OEMs to further improve the robustness of their grid-forming inverter models. These results not only improve the transient stability of these systems but also ensure reliable grid integration as renewable energy resources continue to expand.

# Appendices

## Appendix A1: Derivation of equation (9)

As shown in [4], the active power of a q-CL-VSG can be calculated as

$$P_{\mathrm{VSG},h.n} = 1.5\, v_h\, I_{\mathrm{max},h.n} \cos\left(-\delta_{h.n} - \phi_{\mathrm{sat},h.n}\right). \tag{A1.1}$$

Where $\phi_{\mathrm{sat},h.n} = \cos^{-1}\left(\frac{v_h \sin(\delta_{h.n}-\delta_{\mathrm{v},h})}{I_{\mathrm{max},h.n} Z_{\mathrm{FM},h.n}}\right)$. By letting $P_{\mathrm{VSG},h.n} = P_{0,h.n}$ and re-arranging, the critical value of $v_h$ that makes $P_{\mathrm{VSG},h.n} = P_{0,h.n}$ is derived as

$$V_{\mathrm{c,VSG},h.n} = \frac{P_{0,h.n}}{1.5\, I_{\mathrm{max},h.n}\, cos(-\delta_{h.n}-\phi_{\mathrm{sat}})}. \tag{A1.2}$$

For the GFLIs, their synchronising loop is governed by a PLL, thus to make $v_{\mathrm{FLq},h.m} = 0$

$$V_{\mathrm{c,GFLI},h.m} = \frac{I_{\mathrm{d},h.m} X_{\mathrm{GFLI},h.m} + I_{\mathrm{q},h.m} R_{\mathrm{GFLI},h.m}}{\sin(\theta_{h.m})}, \tag{A1.3}$$

where $I_{\mathrm{d},h.m}$ and $I_{\mathrm{q},h.m}$ are the d- and q-components of GFLI $h.m$'s output current. $X_{\mathrm{GFLI},h.m}$ and $R_{\mathrm{GFLI},h.m}$ are the reactance and resistance components of $Z_{\mathrm{FL},h.m}$.

# Appendix A2: Derivation of equation (10)

Applying the Nodal analysis on the local common bus of cluster $h$ results in

$$\frac{v_h \angle \delta_{\mathrm{v},h} - v_{\mathrm{c}}}{Z_{\mathrm{c},h}} = \left|i_{\mathrm{FL},h.m}\right| \angle \left(\phi_{\mathrm{FL},h.m} + \theta_{h.m}\right) + I_{\mathrm{max},h.n} \angle \left(\phi_{\mathrm{sat},h.n} + \delta_{h.n}\right), \tag{A2.1}$$

where

$$\phi_{\mathrm{sat},h.n} = \cos^{-1}\left(\frac{v_h \sin(\delta_{h.n} - \delta_{\mathrm{v},h})}{I_{\mathrm{max},h.n} Z_{\mathrm{FM},h.n}}\right). \tag{A2.2}$$

Rearranging (A2.1) leads to

$$\begin{aligned} v_h - v_{\mathrm{c}} \angle \left(-\delta_{\mathrm{v},h}\right) \\ = \left|Z_{\mathrm{c},h}\right| \left|i_{\mathrm{FL},h.m}\right| \angle \left(\phi_{\mathrm{FL},h.m} + \theta_{h.m} - \delta_{\mathrm{v},h} + \theta_{\mathrm{Zc},h}\right) \\ + \left|Z_{\mathrm{c},h}\right| I_{\mathrm{max},h.n} \angle \left(\phi_{\mathrm{sat},h.n} + \delta_{h.n} - \delta_{\mathrm{v},h} + \theta_{\mathrm{Zc},h}\right) \end{aligned} \tag{A2.3}$$

where $\theta_{\mathrm{Zc},h}$ is the angle of $Z_{\mathrm{c},h}$. Letting $M = \left|Z_{\mathrm{c},h}\right| \left|i_{\mathrm{FL},h.m}\right|$ and $N = \left|Z_{\mathrm{c},h}\right| I_{\mathrm{max},h.n}$ and decomposing (A2.3) give

$$\sin\left(\delta_{\mathrm{v},h}\right) = \frac{1}{v_{\mathrm{c}}}\left[M \sin\left(\phi_{\mathrm{FL},h.m} + \theta_{h.m} - \delta_{\mathrm{v},h} + \theta_{\mathrm{Zc},h}\right) + N \sin\left(\phi_{\mathrm{sat},h.n} + \delta_{h.n} - \delta_{\mathrm{v},h} + \theta_{\mathrm{Zc},h}\right)\right] \tag{A2.4}$$

and

$$v_h = M \cos\left(\phi_{\mathrm{FL},h.m} + \theta_{h.m} - \delta_{\mathrm{v},h} + \theta_{\mathrm{Zc},h}\right) + N \cos\left(\phi_{\mathrm{sat},h.n} + \delta_{h.n} - \delta_{\mathrm{v},h} + \theta_{\mathrm{Zc},h}\right) + v_{\mathrm{c}} \cos\left(\delta_{\mathrm{v},h}\right). \tag{A2.5}$$

In addition, from (A2.2),

$$v_h = \frac{\cos(\phi_{\mathrm{sat},h.n}) I_{\mathrm{max},h.n} Z_{\mathrm{FM},h.n}}{\sin(\delta_{h.n} - \delta_{\mathrm{v},h})}. \tag{A2.6}$$

Letting $\delta = \delta_{h.n} - \delta_{\mathrm{v},h}$, $\theta = \theta_{h.m} - \delta_{\mathrm{v},h}$ and $\cos\left(\delta_{\mathrm{v},h}\right) = \sqrt{1 - \sin^2\left(\delta_{\mathrm{v},h}\right)}$ in (A2.4), (A2.5), and (A2.6), there are three unknows, i.e., $\delta$, $\theta$, and $\phi_{\mathrm{sat},h.n}$, in the equation system consisting of (A2.4), (A2.5), and (A2.6). By solving this equation system for $\delta$, $\theta$, and $\phi_{\mathrm{sat},h.n}$, and substituting them back into (A2.4) and (A2.5), $v_h$ and $\delta_{\mathrm{v},h}$ can be derived.

# Appendix A3: Derivation of equation (12)

By applying the Nodal analysis on the global common bus, the relations between the global common bus voltage other local common bus voltages can be derive as below,

$$V_{\mathrm{g}} \angle \left(\theta_{\mathrm{g}}\right) = v_{\mathrm{c}} \angle 0 + \sum_{h=1}^{N_{\mathrm{Cl}}} \frac{Z_{\mathrm{g}}}{Z_{\mathrm{c},h}} \left(v_{\mathrm{c}} \angle 0 - v_h \angle \delta_{\mathrm{v},h}\right), \tag{A3.1}$$

where $N_{\mathrm{Cl}}$ is the number of clusters in the system. As there are only two clusters in this study, $N_{\mathrm{Cl}} = 2$. Decomposing (A3.1) leads to the $sin$ and $cos$ component of the grid voltage angle $\theta_{\mathrm{g}}$ as below,

$$\begin{cases} \cos(\theta_{\mathrm{g}}) = \frac{1}{V_{\mathrm{g}}}\left[\sum_{h=1}^{N_{\mathrm{Cl}}=2} \frac{Z_{\mathrm{g}}}{Z_{\mathrm{c},h}}\left(v_{\mathrm{c}} - v_h \cos(\delta_{\mathrm{v},h})\right) + v_{\mathrm{c}}\right] \\ \sin(\theta_{\mathrm{g}}) = -\frac{1}{V_{\mathrm{g}}} \sum_{h=1}^{N_{\mathrm{Cl}}=2} \frac{Z_{\mathrm{g}}}{Z_{\mathrm{c},h}}\, v_h\, \sin(\delta_{\mathrm{v},h}) \end{cases} \tag{A3.2}$$

Eq. (A3.2) is the detailed version of equation (12) in Section 2.5.

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